μ-Helix 3D-antenna technology

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ABSTRACT

This works presents a new MEMS technology for the realization of 3D wire micro-antennas that can be integrated into integrated circuit (IC) packages by means of a layer transfer process. Single antennas or phased arrays are realized as planar structures by metal deposition onto a host silicon wafer over porous silicon areas. The host wafer is then bonded of the IC wafer (over the top metal layer) employing standard wafer-to-wafer bonding processes. The antennas are extruded by pulling the two wafers apart, releasing the metal, and kept in position by injecting a polymer in the gap between the wafers. Host wafer is the de-bonded and the polymer-embedded antennas are exposed. Spiral conical antennas have been designed to operate in the 60 GHz to 1THz frequency ranges to validate the technology. The characteristics of the antennas and of a 16x16 phased square array operating at 960 GHz have been simulated and results are shown.

Keywords: mems, antennas, phased array, porous silicon, IC package.

1 INTRODUCTION

The integration of antenna structures in IC has two main drivers [1]: intra-chip communications, for distributing signals (like low skew clocks) within the IC, on inter-chip communications, to transmit information between chips over free air. In this work, we are interested in the latter kind.

Antenna integration into IC packages, for inter-chip communications, is attractive as it eliminates the need for the design of complex packages with transmission line connections to an external antenna, thus [1] reducing the losses in the signal-to-noise ratio due to the matching network and the external RF components [2]. The matching network, in on-chip antennas can be effectively replaced by tuning antenna impedance to be the conjugate match of the RF frontend circuit [3].

Most integrated antennas implementations, as the one presented in [4], [5], [6] and [7], are planar and realized on the topmost metal layer ([5], [6], [7]) or on a different substrate bonded onto the silicon chip ([4]). Planar antennas can easily be built with standard back-end of line processes and thus they add a little overhead to the final IC cost.

While economical, on-chip antennas, usually, do not show outstanding efficiencies because of the high value of silicon relative permittivity (ε_{Si}=11.7), of the low resistivity (10-20 Ω-cm) of silicon wafers commonly used for CMOS and BiCMOS technologies.

Due to the high value of silicon permittivity, most of the electromagnetic energy radiated by the antenna is coupled to the substrate, if the antenna is laid out near the silicon surface. In [8] is computed that the fraction of radiated power into air for a dipole onto silicon is about 3%. If the antenna is realized over a ground plane onto a dielectric layer (in standard technologies, the dielectric is silicon dioxide), the limited dielectric thickness available lowers the radiation resistance of the antenna, and thus lowers efficiency. The computed radiation resistance of a dipole, for a 15μm thick oxide (a typical for the maximum distance between innermost and topmost metal layers in today's process technologies) is less than 0.1 Ω and this implies that total resistance is dominated by the ohmic losses in the metal and the efficiency is less than 5% [8]. The effect of lossy substrate is discussed in [1] where the radiation efficiency of a dipole (laid on top of 1μm thick oxide, over 670μm of 20 Ω-cm silicon substrate) is reported to be in the 10–15% range. One way to improve efficiency without increasing the substrate resistivity (by changing substrate or proton doping) is to separate the antenna from the substrate as reported in [2] where an example of such antenna in discussed. The technology presented in this work allows to realize 3D metal antennas that can be bonded onto a silicon chip over the topmost metal layer. The antenna is patterned onto a host silicon wafer that will be bonded on the IC wafer. Pulling one wafer keeping the other in place, the antennas are extruded and, once the designed shape is reached, they are kept in position by polymer injection. The host wafer is then de-bonded or etched.

The antennas are embedded in a polymer on top of the silicon wafer. This technology has been demonstrated designing a tapered helical antenna.

2 THE HELICAL-TAPERED ANTENNA

The helical antenna is the basic shape from which the tapered-helical is derived. The helical antenna is generally characterized by high gain, circular polarization and can operate in axial or normal mode. Axial (end-fire) mode of operation is achieved and when the radius "R" (as shown in figure 1) must satisfy the following condition:

$$0.75\frac{c}{2\pi f} < R < 1.33\frac{c}{2\pi f} \quad (1)$$

where c is the speed of light in vacuum and $f = c/\lambda$ is the center frequency.

The spacing "S" between loops determines the input impedance. If $S = \lambda/4$, the antenna impedance $Z_{in} = R_{in} + jX_{in}$ becomes:

$$Z_{in} \cong 140 \frac{2\pi R}{\lambda} \ [\Omega] \tag{2}$$

The impedance can be considered purely resistive, i.e. $R_{in} \gg X_{in}$ if the ratio between the circumference and the wavelength is unitary.

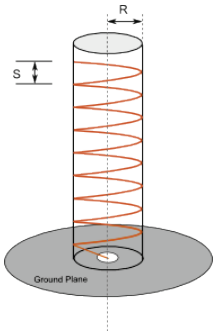

Figure 1: Helical antenna over a ground plane.

The bandwidth of the helical antenna, defined as the frequency span in which the gain is within 1dB of the maximum gain, is limited by the resonance constraint (1) and has frequency ratio of 1.26:1 [9].

Parameter	Description
R_{ext}	External radius of the spiral (see Fig. 3)
R_{int}	Internal radius of the spiral (see Fig. 3)
R_p	Internal pad radius
G	Gap between metal lines
a,b	Width, thickness of metal lines
N	Number of turns
S	Vertical spacing
L	Antenna height

Table 1: Tapered helical antenna design parameters.

2.1 The tapered μ-helix antenna

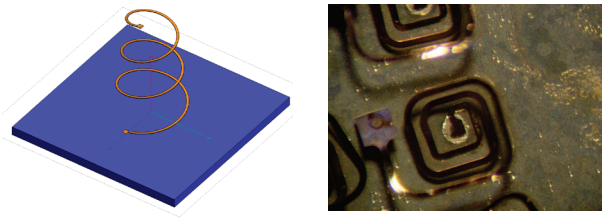

Figure 2: The tapered helical antenna realized with MEMS technology. Drawing (left) and actual sample (right).

According the Rumsey's principle [10], the bandwidth of the antenna can be extended by continuously tapering loops radii. The resulting structure is a cone-shaped helical antenna extruded from a spiral (as shown in figure 2) whose design parameters are summarized in table 1.

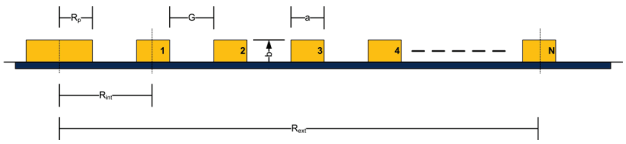

Figure 3: Cross section of the spiral structure from which the antenna is extruded.

The antennas, in this technology, are realized by extrusion from planar shapes. In the case of tapered helical antenna, the wire has the shape of a spiral whose cross section is depicted in figure 3. The numbers within the metal lines represent the number of turns of the spiral and the wider metal line on the left is the internal pad of the spiral.

The external radius R_{ext} is thus computed considering the lower frequency f_l only:

$$0.75 \frac{c}{2\pi f_l} < R_{ext} < 1.33 \frac{c}{2\pi f_l} \tag{3}$$

The internal radius is limited by the technology resolution and must satisfy the following constraint:

$$R_{int} \geq R_{p(\min)} + G_{min} \tag{4}$$

where $R_{p(min)}$ and G_{min} are the minimum pad radius and the minimum gap between the metal lines. The maximum number N_{max} of turns on the antenna are, following (3) and (4):

$$N_{max} = \frac{R_{ext} - R_{int} - 0.5a}{G_{min} + a} \tag{5}$$

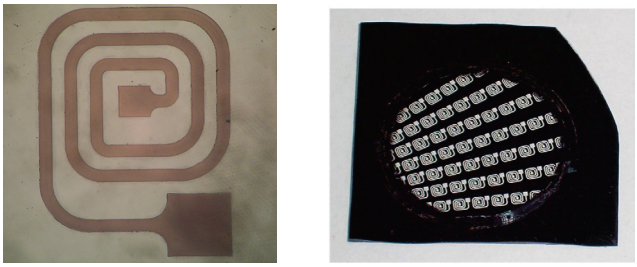

Figure 4: single μ-helix antenna before extrusion (left) and array plating test (right).

The number of turns influences the gain of the antenna and, the more the number of turns, the more the antenna gains. In any case, a minimum value of 3 turns is necessary for the validity of the design equations [11]. The total antenna height is the spacing S between the turns times the number N of turns.

3 THE MEMS TECHNOLOGY

The proposed technology uses materials and process inherited from a MEMS technology [12] to make partially releasable metal structures onto a silicon wafer.

Figure 4 shows a realized antenna (left) prior to extrusion, and the plating test of a circular array (right), whereas figure 5 (below) describes the main technological steps.

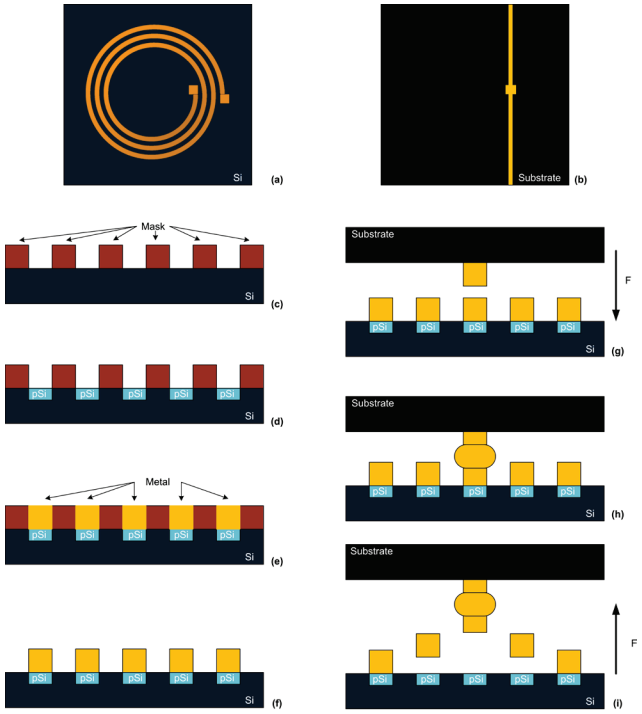

Figure 5: Main technological step to realize the partially releasable structures using a sacrificial porous silicon layer.

In figure 5(a) and 5(b) the top view of an antenna and a substrate with feeding network, respectively, is shown.

The first step is to transfer the pattern of the antenna conductor, as shown in figure 5(c), by photolithography (in this technology wires of 5 to 10 microns wide have been demonstrated [13]). The patterned wafer is then anodized to form a layer of porous silicon, named pSi1 in figure 5(d) that will act as adhesion layer [14] for thick (thickness above 2 μm) metal layers that would delaminate because of internal stresses if, deposited directly on silicon.

The use of porous silicon as adhesion layer allows controlling the force necessary to release the structure from the substrate in subsequent steps, as the porous layer easily breaks when subject to traction [14]. Once the porous layer has been formed, the metal is deposited over the porous silicon as shown in figure 5(e). Metal deposited in a two-step process: first a seed copper layer is deposited by immersion plating [15] and then the thick copper layer that constitutes the antenna conductor is electroplated on top of it. The maximum thickness of the electroplated metal depends on the photoresist thickness. Plating above photoresist thickness alters metal wires section. The mask layer is then removed to expose the metal lines, as depicted in figure 5(f). The extrusion process, needed to create the tridimensional freestanding structure, requires a second substrate (shown in figure 5(b)) onto which anchor pads and feeding structures are realized. This second substrate can be a second silicon wafer, or a different substrate, depending on the application. The silicon wafer and the substrate are aligned onto a wafer/die-bonding machine and pressed. The bonding process will depend on metals and substrate; the only constraint is that the tensile strength of the bond is higher than the one of the pSi1-metal interface so that, during the pulling process, the porous silicon, and not the bond, will break. The bonded assembly, in figure 5(h), is then moved to a pulling machine for the extrusion of the antenna. The extrusion consists in pulling away one substrate from the other controlling the total displacement. In the pulling process, the metal wires are partially released from the host silicon wafer and are kept in position by the two pads, one on the porous silicon on host wafer and the other one on the second substrate (figure 5(i)).

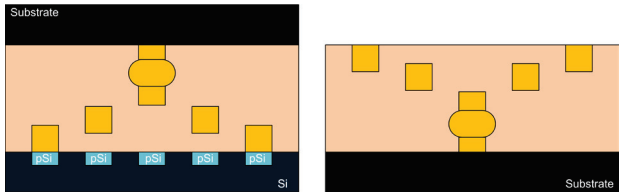

Figure 6: Antenna finalization: a polymer is injected (left) and the silicon host wafer is de-bonded.

The space between the wafer and the substrate is then filled with a transparent polymer to keep the metal wires in position as shown in figure 6 (left). The silicon wafer can be de-bonded or removed (figure 6, right), if necessary, by dry etch (Reactive Ion Etch or XeF_2 etch) or wet etch (TMAH etch) to expose the antenna structure.

4 ANTENNA SIMULATIONS

Antenna structures operating in the 60 GHz to 1 THz band have been simulated to asses performances of practical structures.

Parameter	60 GHz	220 GHz	770 GHz
R_{ext}	1320 μm	295 μm	95 μm
R_{int}	75 μm	45 μm	30 μm
R_p	75 μm	5 μm	5 μm
G	25 μm	25 μm	10 μm
a,b	150, 10 μm	10, 5 μm	10, 5 μm
N	6	7	3
S	1500 μm	380 μm	127 μm
L	9370 μm	2660 μm	380 μm

Table 2: μ-helix structures design for three different bands of operation.

The dimensional characteristics of the simulated antennas are summarized in table 2. Single antenna simulations have been carried on 4NEC2 free simulator placing the antenna over an infinite ground plane. The figure of merit are the S11, the input impedance ($Z_{in} = R_{in} + jX_{in}$), the voltage standing wave ratio (VSWR) computed on a 150 Ω reference impedance, the total gain and the 3dB-beamwidth (FWHM, full width at half maximum).

Parameter	60 GHz	220 GHz	770 GHz
f_l [GHz]	56	220	613
f_h [GHz]	72	260	924
S11 [dB]	-6	< -10	< -18
R_{in} [Ω]	88	160	140
X_{in} [Ω]	-110	-100 to -70	-35 to +20
VSWR	<3 (150Ω)	<1.8 (150 Ω)	<1.3 (150Ω)
Gain [dBi]	6 to 7	5.5 to 8.5	3 to 5.5
FWHM	< 70°	< 70°	<70°

Table 3: Single antenna performances from 4NEC2 simulations.

The results of simulations have been reported in table 3 where the bandwidth of the antenna is given by the difference $f_h - f_l$ and is defined by the requirements of having a FWHM < 70° and a S11 <-10dB. The 60 GHz antenna lower performances establish that frequency as limit for the presented design procedure but does not constitues a limit of the technology.

The 770 GHz antenna has been further optimized (varying the S parameter) in FEKO(R) to radiate at 960 GHz and used to design 16x16 square phased array laid over a 20μm layer of SiO_2. The array, simulated with FEKO(R) has a maximum gain of 38.5 dBi with -13 dB sidelobe level and a FVHM of 5.4°. The radiation pattern is shown in figure 7.

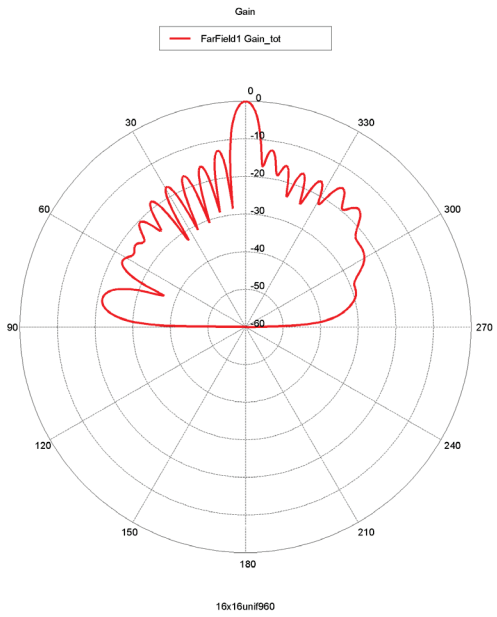

Figure 7: 16x16 array radiation pattern.

5 CONCLUSIONS

In this work a new technology for three dimensional antenna integration into IC package has been presented. The main advantage of the technology is the use of standard back-end of line processes for the realization of structures. Tapered helical antenna design, in the 60-1000 GHz frequency range, have been simulated to asses antenna performance that shows good performances above 60 GHz. An optimized antenna has been used to design a 960 GHz 16x16 phased array that can be integrated into an IC package.

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