FinFET Reliability Issue Analysis by Forward Gated-Diode Method

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ABSTRACT

The reliability issue of the FinFET device is studied in details in this paper by the forward gated-diode R-G current method. Extraction of the stress induced interface states and oxide traps of FINFET is performed from a series of the R-G current measurement and developed physics expression. As the result, the interface states can be extracted by the relationship between the net increase value of the maximum substrate current (Δ Ipeak) and stress time; and the oxide trap can be reflected by the drift of gate voltage (Δ Vg) corresponding to Δ Ipeak.

Keywords: FinFET, R-G current, stress, interface state, oxide trap, reliability issue.

Ⅰ INTRODUCTION

The multi-gate MOSFET is considered to be one of the most promising device architectures for scaling CMOS to the 45-nm technology node and beyond [1]–[5]. Improved short-channel effects (SCEs), and equivalent current drivability to planar CMOS, can be expected from these devices. The FINFET architecture has emerged as one of the most successful methods [6] for fabricating double-gate [7], triple-gate [8], and the circuits formed by FINFET also show very promising results.

However, the performance of such nano-scaled devices is seriously suffered from traps in the gate oxide and the interface between Si field and SiO2[9]. It has been reported that the application of forward gate-diode R-G current to analyze the stress-induced interface and oxide traps of SOI MOSFET is a very useful, simple, sensitive and flexible method.

In this paper, we presented analysis of the gate voltage-induced-traps of FINFET by using this method. First, the principle of forward gated-diode R-G current method is simple introduced. Then, the measurement and analysis of stress induced interface states and oxide traps of FINFET.

Ⅱ MEASURMENT AND ANALYSIS OF STRESS INDUCED INTERFACE STATE AND OXIDE TRAP OF FINFET

Recently, a refined forward gated-diode method has been used to characterize the interface traps and extract the bulk carrier recombination lifetime in the SOI devices by extracting recombination–generation (R–G) current,. The principle and some results has been reported in references [9-10]. This method is also useful to the extraction of interface states and oxide traps of FINFET.

The total diode current is the sum of the interface R-G current, bulk R-G current and the bulk diffusion current for all biasing states

$$I_{total} = I_{R-G(sur)} + I_{R-G(bulk)} + I_{diffusion} \tag{1}$$

No matter the gated-diode under forward bias or reward bias, the bulk R-G current IR-G(bulk) could be neglected and R-G current is the significant part of the total current. Scan the gate voltage range from negative bias to positive bias (which due to the channel under gate changes from accumulation to depletion) by keeping bias on the gate-diode constantly, changes of surface potential and carrier concentration can be observed except the diffusion. R-G current rises to a peak point first and then decreases to a constant level. The maximum R-G current (I_{peak}) can be determined by equation $\frac{\partial F}{\partial n} = 0$, and Ipeak could be expressed as

$$I_{peak} = \frac{1}{2} q n_i (c_n c_p)^{1/2} N_{it} WL \exp(\frac{qV_b}{2kT}) \tag{2}$$

$$c_n = c_p = 10^{-8} cm^{-3} s^{-1}$$

Therefore, a peak point of R-G current can be achieved from Equation (2).

In this section, gate-diode R-G current method has

been used in FINFET to extracting and distinguishing the Si/SiO2 interface states and oxide traps. The 3-D structure and layout of the FINFET we tested are shown in Fig.1, which were made from the fabrication process line of the Institute of Microelectronics, Peking University.

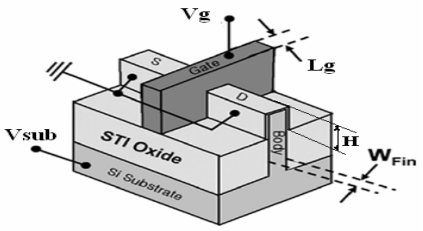

Fig.1. 3-D Structure of FINFET

As shown in Fig.1, Lg is the length of the channel, WFin is the width of the Si body and H is the height of the Si body. Vg and Vsub are added to the gate and substrate, respectively. Source and drain are always grounded during the measurement.

A. Analysis of Interface State and Oxide Trap

In the measurement, the source and drain are connected to ground while applying a constant low biased voltage Vb to the body contact. As a result, the source/drain and body contact formed a forward diode. Based on the principle discussed in section Ⅱ, by scanning the gate voltage from negative bias to positive bias (which due to the channel under gate changes from accumulation to depletion), the R-G current due to the interface states and oxide traps could be obtained. The gate voltage stress is set to be 3V and the accumulated stress time is changed from 0s, through 10s, 20s, 50s, 80s, 100s, 200s, 500s, 800s, 1000s, finally to 2000s. The R-G current characteristics of the devices were automatically recorded by a semiconductor parameter analyzer HP-4156B after stress duration.

The bias conditions we used in our measurement are exhibited as follows: (1). To prevent the forward diode formed by the drain and body from turning on, Vb is set to range from 0.4V to 0.5V with the step of 0.01V. (2). V_g ranges from -0.4V to 0.4V and the peak value of the substrate current (I_b) must be ensured in this voltage area.

Fig.2 shows the relationship of I_b and V_g with the variation of V_b without stress.

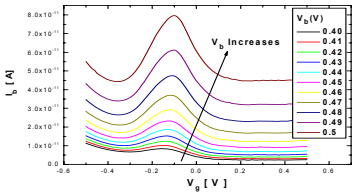

Fig.2. I_b vs V_g under different V_b without stress

From Equation (2), we could obtain

$$\ln I_{peak} = \ln[\frac{1}{2} q n_i (c_n c_p)^{1/2}] + \ln(N_{it} WL) + \frac{qV_b}{2kT} \qquad (3)$$

Fig.3. shows the experiment curve of the maximum I_b (I_{peak}) versus V_b and fitted linearly by the equation y=A+Bx.

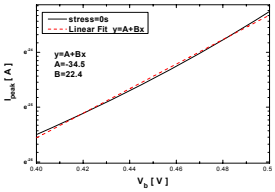

Fig.3. The experiment curve and the linearly fit curve of I_{peak}—V_b, with fit parameters A=-34.5，B=22.4

From Equation(3), *A* and *B* can be written as

$$A = \ln[\frac{1}{2} q n_i (c_n c_p)^{1/2}] + \ln(N_{it} WL), \quad B = \frac{q}{2kT}$$

By linear fitting, we got $\ln(N_{it} WL) = -7.08$.

Because the performance of a FINFET is equal to a double gate MOSFET, which means that the factor WL in parameter A is determined by the gates at both sides of the Si film. Assuming that the Si/SiO_2 interface states density N_{it} is equal to the normal value about $5\times10^{10} cm^{-2}$. According to Equation (3), the product of Si body height (corresponding to the channel width) and the effective gate length (WL) is equal to 67.2nm^2.

The relationship between the substrate current I_b and gate voltage V_g under different stress time by keeping V_b=0.5V is shown in Fig.4. An increase of I_b with increasing stress time is observed. In Fig.6, the slops of all the I_{peak}-V_b curves are almost the same, and the value is about *q/2kT*, which corresponds to Equation (3) very well. Meanwhile, the increase of the interface states density N_{it} with increased stress time is reflected by the increasing of the intercept of I_{peak}-V_b curves as shown in Fig.5. The differences of intercept under stresses between the fresh one implies the interface states induced by the stress. The dependence of ΔI_{peak} and interface states distribution to the stress time is

shown in Fig.6 and Fig.7. From Fig.7 we can get the relationship between net increased N_{it} (ΔN_{it}) and stress time (t) is $\Delta N_{it} \propto t^{0.39}$.

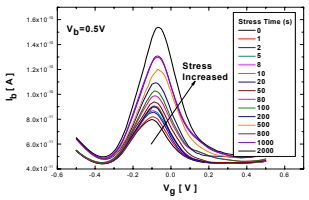

Fig.4. I_b versus V_g characteristics under different stress time

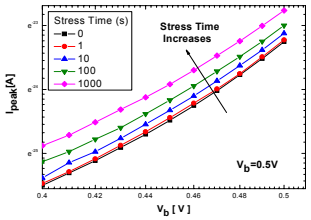

Fig.5. I_{peak} versus V_b characteristics under different stress time

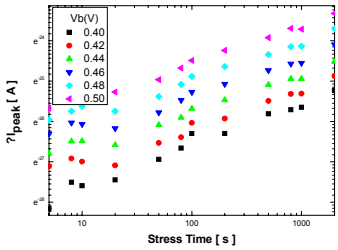

Fig.6. ΔI_{peak} versus stress time under different V_b

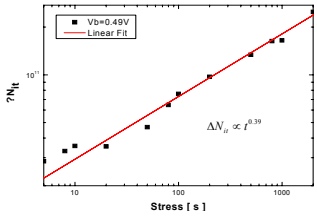

Fig.7. the dependence of the interface states distribution to the stress time

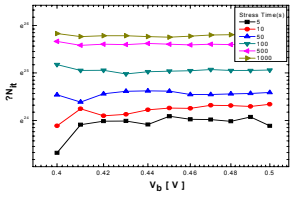

Fig.8. The generation of interface state versus V_b under different stress time

Fig.8 shows the relationship between the interface state generation and V_b under different stress time. We can observe that the generation of interface states increases with the stress time but almost independent of V_b. This phenomenon implies that the front gate interface is less affected by the increasing V_b. The increased V_b just supply more carriers which reacted with the interface states to generate larger substrate current (I_b). So under a constant stress situation, the drift of the peak value in I_b-V_g characteristics with different V_b (i.e. Fig.2) is determined only by the charge in the oxide, so the oxide charge density under some stress could be extracted by the drift of I_{peak} following this equation

$$\Delta V = C_{ox} Q_{ox} \tag{9}$$

Where ΔV is the difference between the V_b corresponding to the drifted I_{peak}, C_{ox} is the capacitance of the gate oxide, and Q_{ox} is charges trapped by the oxide traps.

B. Hot carrier induced interface state and oxide trap

Hot carrier due to the high electrical field near the drain area will induce the interface states and oxide trap. In order to analyze the trap generation induced by the hot carrier effect, we add the stress to the device under the condition of V_d=3.5V， V_g=1.11V, so that the largest substrate current I_b could be observed. And the stress time ranges from 0s, through 10s, 20s, 50s, 80s, 100s, 200s, 500s, 800s, finally to 1000s. In this section, we focus our attention on the degradation of I-V characteristics to analyze the interface state and oxide trap.

Fig.9 is the I_b-V_g characteristic without stress. It is shown in Fig.9 that I_b increasing with increased V_b before stress. But voltage corresponding to the peak of I_b is almost steady. So we can conclusion that the increase of V_b just supplies larger recombine current but does not generate interface states or oxide traps which induce the degradation of the sub threshold slop and threshold voltage. Fig.10 is the I_b-V_g characteristic under different stress time. The increasing of I_b with increased stress time can be observed. And the drift of I_{peak} resulted from the charges in the oxide is also observed in Fig.10.

The experiment and linear fit line of the difference between I_{peak} under different stress and initial I_{peak0} without stress versus stress time is shown in Fig.11 and Fig.12.

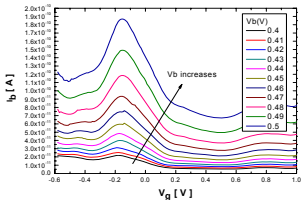

Fig.9. I_b-V_g characteristic without stress

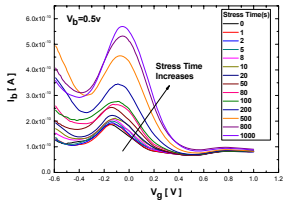

Fig.10. I_b-V_g characteristic under different stress time

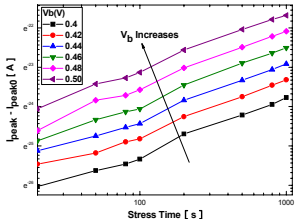

Fig.11. The relationship between ΔI_{peak} and stress time with different V_b

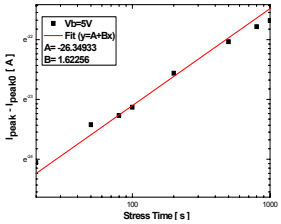

Fig.12. Linear fit of ΔI_{peak} versus stress time.

III CONCLUSION

In this paper, the Si/SiO_2 interface state and oxide trap of FINFET are discussed. Gate-diode R-G current method is used for extracting and distinguishing these two types of traps induced by stress. The interface states can be extracted by the relationship between the net increase value of the maximum substrate current (ΔI_{peak}) and stress time; and the oxide trap can be reflected by the drift of gate voltage (ΔV_g) corresponding to ΔI_{peak}. During the studying of the hot carrier induced interface and oxide traps, we found that the I_d-V_d and I_s-V_s characteristics degrade due to hot carrier stress induced defects in the interface and oxide.

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