

Simulation of Field-Plate Effects on Surface-State-Related Lag and Current Slump in GaAs FETs

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ABSTRACT

Two-dimensional transient analysis of field-plate GaAs MESFETs is performed in which surface states are considered. Quasi-pulsed current-voltage curves are derived from the transient characteristics. It is shown that drain lag and current slump due to surface states are reduced by introducing a field plate because fixed potential at the field plate leads to reducing trapping effects by the surface states. Dependence of lag phenomena and current slump on field-plate length and SiO₂ passivation layer thickness is also studied, suggesting that there are adequate values of field-plate length and SiO₂ layer thickness to reduce current slump and also to maintain high-frequency performance of GaAs FETs.

Keywords: GaAs FET, current slump, drain lag, gate lag, surface state

1 INTRODUCTION

In compound semiconductor FETs, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [1,2]. This is called drain lag or gate lag, and undesirable for circuit applications. Slow transients indicate that dc and RF current-voltage (I - V) curves become quite different, resulting in lower RF power available than that expected from dc operation [3]. This is called current slump. These phenomena occur due to surface states and/or bulk traps [1-5]. Experimentally, the introduction of field plate like Fig.1 is shown to reduce the lags and current slump [3,6,7]. However, few simulation studies on field-plate structures have been made, although GaN-based FETs with bulk traps are studied [8]. Therefore, in this work, we have made two-dimensional transient simulation of field-plate GaAs MESFETs including surface states, and found that surface-related lags and current slump can be reduced by introducing a field plate.

2 PHYSICAL MODEL

Fig.1 shows a device structure analyzed in this study. The gate length L_G is typically set to $0.3 \mu\text{m}$. The gate electrode extends on to SiO₂ passivation layer. This is called a field plate. The field-plate length L_{FP} is varied as a parameter. The thickness of SiO₂ layer d is also varied. Surface states are considered on the planes between the

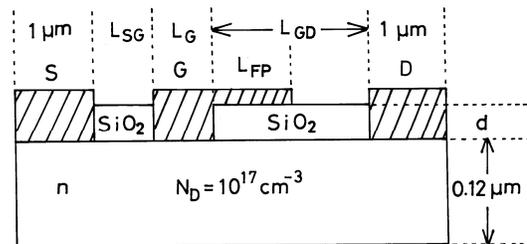


Figure 1: Device structure analyzed in this study.

source and the gate and on the planes between the gate and the drain. As a surface-state model, we adopt Spicer's unified defect model, and assume that the surface states consist of a pair of a deep donor and a deep acceptor. The surface states are assumed to distribute uniformly within 5 Å from the surface, and their densities (N_{SD} , N_{DA}) are typically set to $2.5 \times 10^{19} \text{ cm}^{-3}$ ($1.25 \times 10^{12} \text{ cm}^{-2}$). As for their energy levels, the following case based on experiments is considered as in a previous work [9]: $E_{SD} = 0.87 \text{ eV}$, $E_{SA} = 0.7 \text{ eV}$, where E_{SD} is the energy difference between the bottom of conduction band and the deep donor's energy level, and E_{SA} is the energy difference between the deep acceptor's energy level and the top of valence band. In this case, the deep-acceptor surface state mainly determines the surface Fermi level, and it acts as a hole trap.

Basic equations to be solved are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels [9,10]. These equations are put into discrete forms, and are solved numerically. We calculate the drain-current responses when the drain voltage V_D and/or the gate voltage V_G are changed abruptly.

3 SLOW CURRENT TRANSIENT

Fig.2 shows calculated drain-current responses of GaAs MESFETs considering surface states when V_D is lowered abruptly from 10 V to V_{Dfm} , where V_G is kept constant at 0 V. Fig.2(a) is for a case without a field plate, and Fig.2(b) is for a case with a field plate ($L_{FP} = 1 \mu\text{m}$). The thickness of SiO₂ layer d is $0.1 \mu\text{m}$. In both cases, the drain currents remain at low values for some periods ($10^{-10} - 10^{-1} \text{ s}$) and begin to increase slowly, showing drain lag behavior. It is understood that the drain currents begin to increase when

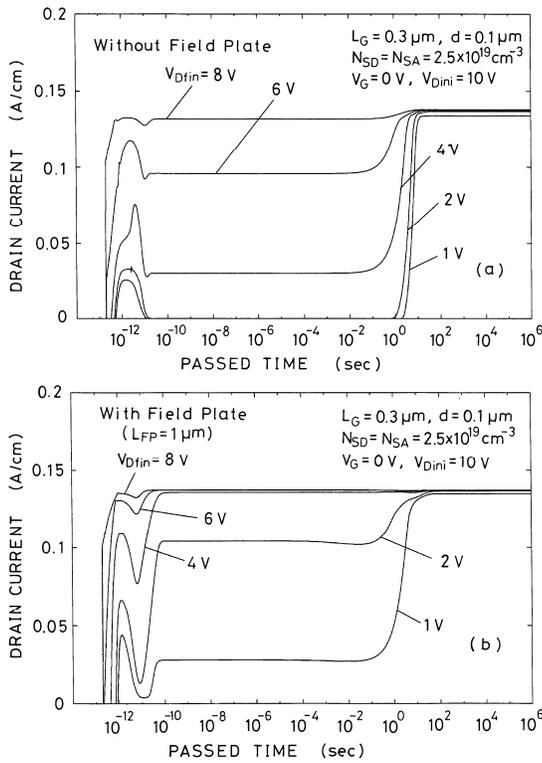


Figure 2: Calculated drain-current responses of GaAs MESFETs with surface states when V_D is lowered abruptly from 10 V to V_{Dfin} , while V_G is kept constant at 0 V. $N_{SD} = N_{SA} = 2.5 \times 10^{19} \text{ cm}^{-3}$. (a) Without field plate, (b) with field plate ($L_{FP} = 1 \mu\text{m}$, $d = 0.1 \mu\text{m}$).

the deep-acceptor surface states begin to capture holes [10] or emit electrons. It is clearly seen that the change of drain current is smaller for the case with a field plate when comparing for the same V_{Dfin} , indicating that the drain lag is smaller for the field-plate structure. We will discuss below why this happens.

Fig.3 and Fig.4 show potential profiles during the transients for the cases without a field plate and with a field plate, respectively when V_D is changed from 10 V to 2 V. Please note that the vertical axis is $-\psi$. Figs.3(a) and 4(a) ($t = 0$) are profiles before V_D is changed, that is, for $V_D = 10$ V. Figs.3(b) and 4(b) are profiles at $t = 10^{-9}$ s after V_D is changed, and Figs.3(c) and 4(c) are profiles at $t = 10^{-2}$ sec after V_D is changed. (Please note that during $10^{-9} - 10^{-2}$ s, the drain currents remain at constant values (lower than the steady-state values), and hence Fig.3(b) (Fig.4(b)) and Fig.3(c) (Fig.4(c)) become essentially the same.) Figs.3(d) and 4(d) ($t = 10^6$ s) correspond to steady-state profiles ($V_D = 2$ V). From Figs.3(b) and 3(c), we see that without a field plate, electron energies ($-e\psi$) become rather high between gate and drain region, and an energy barrier for electrons is formed toward the drain. Therefore, the drain current remains at almost zero during $10^{-9} - 10^{-2}$ s, as seen in Fig.2(a) ($V_{Dfin} = 2$ V). It is understood that this barrier vanishes when the surface states between the gate and the

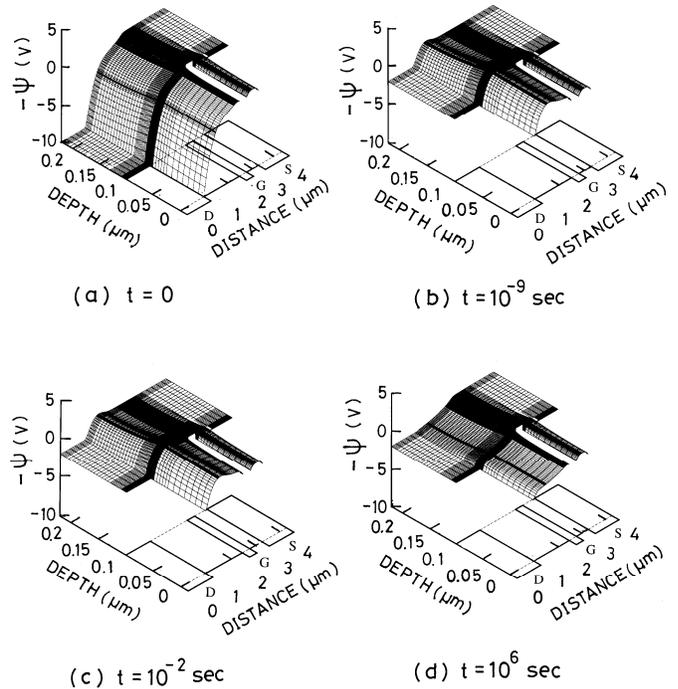


Figure 3: Change of potential profiles with time t when V_D is lowered from 10 V to 2 V for the case without a field plate, corresponding to Fig.2(a). $d = 0.1 \mu\text{m}$.

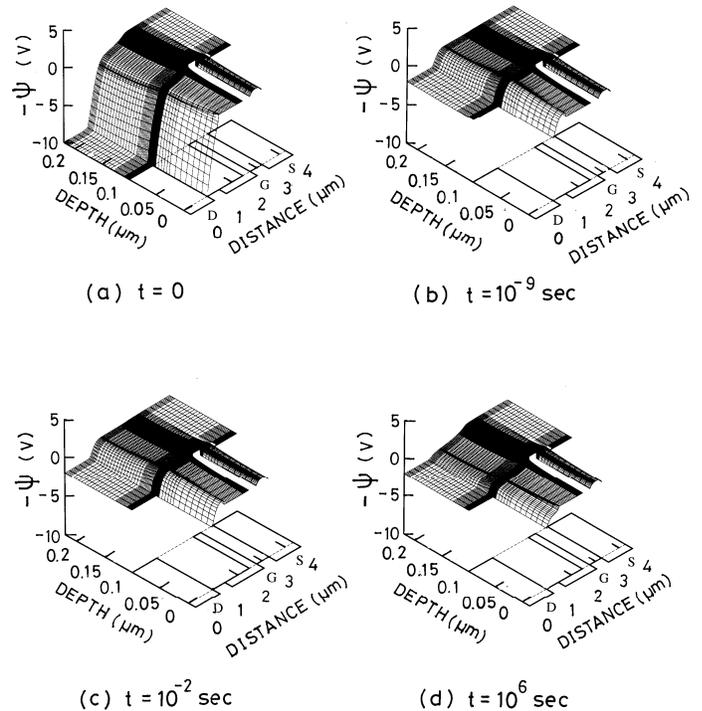


Figure 4: Change of potential profiles with time t when V_D is lowered from 10 V to 2 V for the case with a field plate, corresponding to Fig.2(b). $L_{FP} = 1 \mu\text{m}$, $d = 0.1 \mu\text{m}$.

drain respond (see Fig.3(d)). On the other hand, with a field plate, the potential profiles or electron energy profiles are almost flat at the semiconductor region under the field plate, as seen in Figs.4(b) and 4(c). This is because the field plate exists on the SiO₂ layer and the potential there is fixed. Some energy barrier is seen at the drain side, and hence the drain current remains at a lower value than the steady-state one during 10⁻⁹ – 10⁻² s, as seen in Fig.2(b) ($V_{Dfm} = 2$ V). But, it can be said that the drain lag is greatly reduced by introducing a field plate.

4 CURRENT SLUMP

Next, we have calculated a case when V_G is also changed from an off point. V_G is changed from the threshold voltage V_{th} to 0 V, and V_D is lowered from 10 V to V_{Don} (on-state drain voltage). V_{th} is defined here as a gate voltage where the drain current I_D becomes 5×10^{-3} A/cm. The characteristics (not shown here) become similar to those in Fig.2, although some transients arise when only V_G is changed (gate lag). From these turn-on characteristics, we obtain a quasi-pulsed $I-V$ curve.

In Fig.5, we plot by (x) the drain current at $t = 10^{-8}$ sec after V_G is switched on, with V_{Don} (V_D) as a parameter. Fig.5(a) is for the case without a field plate, and Fig.5(b) is for the field-plate structure ($L_{FP} = 1 \mu\text{m}$, $d = 0.1 \mu\text{m}$). These curves are regarded as quasi-pulsed $I-V$ curves with pulse width of 10^{-8} sec. Without a field plate, the pulsed $I-V$ curve lies significantly lower than the steady-state $I-V$ curve (solid line), indicating current slump and gate lag behavior. In Fig.5, we also plot another pulsed $I-V$ curve (Δ), which is obtained from Fig.2 (when only V_D is changed), indicating large drain lag without a field plate. However, from Fig.5(b), we can definitely say that by introducing a field plate, the current slump, drain lag and gate lag are greatly reduced. Particularly, the reduction of drain lag is contributing to reducing the current slump in this case.

5 FIELD-PLATE PARAMETER DEPENDENCE

We have next studied dependence of lag phenomena and current slump on the field-plate length L_{FP} and on the SiO₂ thickness d .

Fig.6 shows drain current reduction rate $\Delta I_D/I_D$ (ΔI_D : current reduction, I_D : steady-state current) due to current slump, drain lag or gate lag, with L_{FP} as a parameter. Here, $d = 0.1 \mu\text{m}$. The values of current slump and drain lag are taken from the case when V_D is lowered from 10 V to 2 V. It is seen that when L_{FP} becomes long ($\geq 0.8 \mu\text{m}$), the drain lag and current slump become reduced. This is because for longer L_{FP} , the energy barrier between field-plate edge and drain, which is formed when V_D is lowered, becomes smaller as was shown in Figs.4(b) and 4(c). In the case when V_D is lowered from 10 V to 4 V, the reduction in drain lag and current slump starts at shorter L_{FP} .

Fig.7 shows the drain-current reduction rate $\Delta I_D/I_D$ due

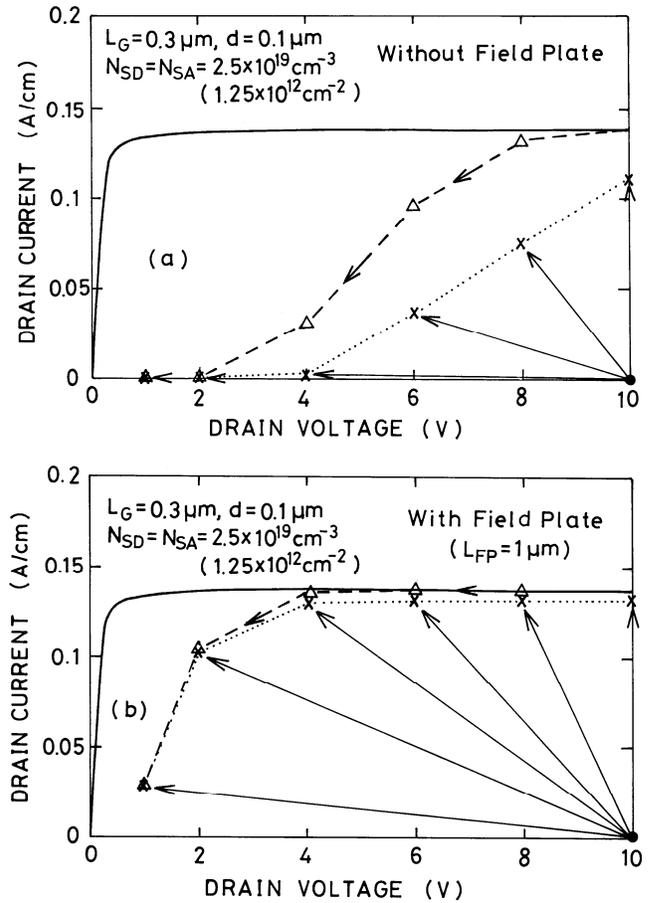


Figure 5: Steady-state $I-V$ curves ($V_G = 0$ V; solid lines) and quasi-pulsed $I-V$ curves (Δ , x) of GaAs MESFETs with surface states. (a) Without field plate, (b) with 1 μm -length field plate. $d = 0.1 \mu\text{m}$. (Δ): Only V_D is changed from 10 V ($t = 10^{-8}$ sec), (x): V_D is lowered from 10 V and V_G is changed from V_{th} to 0 V ($t = 10^{-8}$ sec).

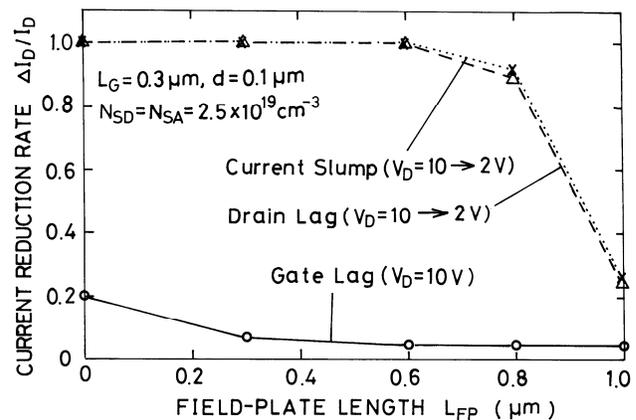


Figure 6: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with field plate length L_{FP} as a parameter. $d = 0.1 \mu\text{m}$. $N_{SD} = N_{SA} = 2.5 \times 10^{19} \text{ cm}^{-3}$.

to current slump, drain lag or gate lag, with d as a parameter. Here, $L_{FP} = 1 \mu\text{m}$. It is seen that when d is thick, the current slump and drain lag are relatively large. This is because for thick d , the existence of field plate does not almost affect the characteristics. For moderate d , the current slump and drain lag are reduced greatly. This is because the surface state-related effects are reduced as described in section 3. However, for thin d , the current slump and drain lag increase steeply. This may be because in such a case, the field plate becomes acting like a gate electrode. From this figure, it can be said that there is an optimum thickness of SiO_2 layer to minimize the surface state-related current slump and drain lag in GaAs FETs.

From Fig.6, it can be said that to reduce the current slump and drain lag in the field-plate GaAs MESFETs, L_{FP} should be longer. However, when L_{FP} is long and d is thin, the gate (parasitic) capacitance becomes large and the high frequency characteristics may degrade. Therefore, it is suggested that there are adequate values of L_{FP} and d to reduce the current slump and also to maintain the high frequency performance of GaAs FETs.

6 CONCLUSION

Two-dimensional transient simulations of the field-plate GaAs MESFETs have been performed in which surface states are considered. Quasi-pulsed I - V curves have been derived from the transient characteristics.

It has been shown that the drain lag, gate lag and current slump due to surface states are reduced by introducing a field plate. This is because fixed potential at the field plate leads to a smaller energy barrier formed between gate and drain during the transients. It has also been shown that the current slump due to surface states becomes smaller for longer field plate and for moderate SiO_2 thickness.

It is suggested that there may be optimum values for the field-plate length and SiO_2 layer thickness to reduce the current slump and also to maintain the high-frequency performance of GaAs FETs. In order to determine the optimum values, more works are needed concerning estimation of the real power performance together with the frequency characteristics.

REFERENCES

- [1] J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with improved breakdown voltage for X - and Ku -band power applications", IEEE Trans. Microwave Theory Tech. 41, 752, 1993.
- [2] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs", Proc. IEEE 90, 1048, 2002.
- [3] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers", Proc. IEEE 96, 287, 2008.

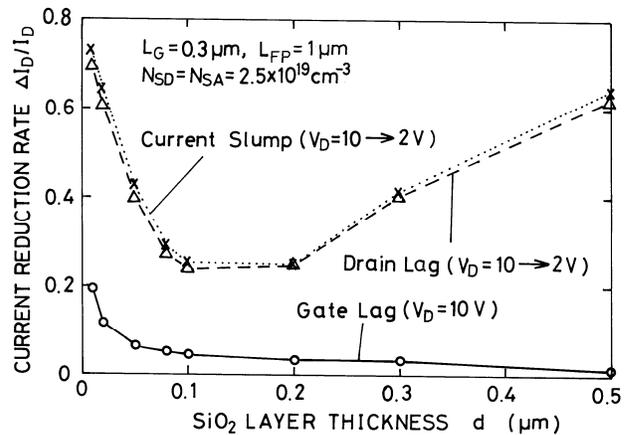


Figure 7: Current reduction rate $\Delta I_D/I_D$ due to current slump, drain lag or gate lag for GaAs MESFETs, with SiO_2 thickness d as a parameter. $L_{FP} = 1 \mu\text{m}$. $N_{SD} = N_{SA} = 2.5 \times 10^{19} \text{cm}^{-3}$.

- [4] G. Koley, V. Tilak, L. F. Eastman and M. G. Spencer, "Slow transients observed in AlGaIn/GaN HFETs: Effects of SiN_x passivation and UV illumination", IEEE Trans. Electron Devices 50, 886, 2003.
- [5] V. Desmaris, M. Rudzinski, N. Rorsman, P. R. Hageman, P. K. Larsen, H. Zirath, T. C. Rodle, and H. F. F. Jos, "Comparison of the dc and microwave performance of AlGaIn/GaN HEMTs grown on SiC by MOCVD with Fe-doped or unintentionally doped GaN buffer layers", IEEE Trans. Electron Devices 53, 2413, 2006.
- [6] A. Koudymov, V. Adivarahan, J. Yang, G. Simon and M. A. Khan, "Mechanism of current collapse removal in field-plated nitride HFETs", IEEE Electron Device Lett. 26, 704, 2005.
- [7] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure", IEEE Trans. Electron Devices 54, 1825, 2007.
- [8] K. Horio, A. Nakajima, and K. Itagaki, "Analysis of field-plate effects on buffer-related lag phenomena and current collapse in GaN MESFETs and AlGaIn/GaN HEMTs", Semicond. Sci. Technol. 24, 085022, 2009.
- [9] Y. Kazami, D. Kasai, and K. Horio, "Numerical analysis of slow current transients and power compression in GaAs FETs", IEEE Trans. Electron Devices 51, 1760, 2004.
- [10] K. Horio and T. Yamada, "Two-dimensional analysis of surface-state effects on turn-on characteristics in GaAs MESFET's", IEEE Trans. Electron Devices 46, 648, 1999.