Characterization and Modeling of Metal Finger Capacitors

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ABSTRACT

An interdigitated metal finger capacitor is a device of low cost, high capacitance density, superior voltage linearity, and high quality factor. We present a method of systematically characterizing and modeling the capacitance and resistance of metal finger capacitors. It includes a scalable capacitance model for metal finger capacitors made of same metal levels and a set of capacitance relations for metal finger capacitors consisting of different metal levels in a semiconductor technology. We also discuss how to maximize the quality factor of a metal finger capacitor.

Keywords: Metal finger capacitor, vertical native back-end-of-line (BEOL) capacitor, SPICE model, passive device modeling, capacitance modeling, resistance modeling.

1 INTRODUCTION

A capacitor solution with no mask or process additions can be formed by the use of interdigitated metal fingers. Often, this metal finger capacitor uses multiple back-end-of-line (BEOL) levels to increase capacitance density [1,2]. Metal structures at different BEOL levels are connected using vias between tabs, and vias may also directly connect fingers of two adjacent BEOL levels (Fig. 1). Metal finger capacitors are used in a variety of VLSI circuits (e.g., analog-to-digital converters). We discuss the characterization and modeling of metal finger capacitors and show a more accurate approach to extract capacitance density from measured data or from a SPICE model of a metal finger capacitor. When technology rules allow a metal finger capacitor to use the first K BEOL levels of a semiconductor technology, we first show a set of capacitance relations, and then show a smarter way to cover $K(K+1)/2$ possible level combinations of the metal finger capacitor using only $(2K-1)$ level combinations in semiconductor physical test structures (testsite). We present a compact model of metal finger capacitors, which include various capacitance components (electric field lines in via space, field lines above the top level of a capacitor, and field lines below the bottom level of a capacitor) and the modeling of the total resistance of the capacitor.

2 CAPACITANCE CHARACTERIZATION

For a given set of metal levels, capacitance scalable model [vs. device design length (L) and design width (W)] is

$$C = c_a LW + 2c_l L + 2c_w W + c_0 , \quad (1)$$

where c_a is an area density, c_l and c_w are two perimeter densities, and c_0 is a constant. A typical characterization method is to measure the total capacitance C for a large design dimension LxW, and then set $c_a = C/(LW)$. A more accurate method, however, is first to design and fabricate a set of four device sizes (L_1xW_1, L_1xW_2, L_2xW_1, and L_2xW_2) for the given set of metal levels, then to measure the total capacitances (C_{11}, C_{12}, C_{21}, and C_{22}) of the four sizes, and last to extract capacitance density using Eq. (1),

$$c_a = (C_{11} - C_{12} - C_{21} + C_{22}) / [(L_1 - L_2)(W_1 - W_2)]. \quad (2a)$$

Perimeter densities c_l and c_w can be extracted similarly,

$$c_l = \frac{C_{11} - C_{21}}{2(L_1 - L_2)} - \frac{c_a W_1}{2}, \qquad c_w = \frac{C_{11} - C_{12}}{2(W_1 - W_2)} - \frac{c_a L_1}{2}. \quad (2b)$$

3 CAPACITANCE RELATIONS

There exist some relations among capacitance densities for different level combinations. For example,

$$\begin{aligned} & c_a(\mathrm{M1+M2+M3}) + c_a(\mathrm{M2}) \\ & = c_a(\mathrm{M1+M2}) + c_a(\mathrm{M2+M3}), \end{aligned} \quad (3)$$

where c_a(M1+M2+M3) refers to the capacitance density for a capacitor using metal levels M1, M2, and M3, etc. On the other hand, some naïve relations do not hold in general. For example, even when the finger width, finger space, metal thickness, and inter-finger dielectric material for M2 level are identical to those for M3 level and when the heights and dielectric materials for V1 (via between M1 and M2 metal levels), V2, and V3 are all identical, the following symmetry breaking relation exists,

$$c_a(\mathrm{M2+M3}) \neq c_a(\mathrm{M2}) + c_a(\mathrm{M3}). \quad (4)$$

We first explain inequality (4). The capacitance density c_a(M2) for a single M2 level capacitor comprises three components: the capacitance between the bottom faces of neighboring M2 fingers (due to the electric field lines below the bottom faces of M2 fingers), c_a(M2 bottom); the capacitance between the side walls of neighboring M2 fingers, c_a(M2-M2); and the capacitance between the top faces of neighboring M2 fingers, c_a(M2 top). The capacitance density c_a(M3) for another single M3 level capacitor also comprises three components: the capacitance between the bottom faces of neighboring M3 fingers, c_a(M3 bottom); the capacitance between the side walls of neighboring M3 fingers, c_a(M3-M3); and the capacitance between the top faces of neighboring M3 fingers, c_a(M3 top). So the sum of c_a(M2) and c_a(M2) consists of six components. One the other hand, the capacitance density c_a(M2+M3) for a capacitor consisting of M2 and M3 two metal levels contains five components: c_a(M2 bottom), c_a(M2-M2); a capacitance component due to the electric field lines in the space of via V2, c_a(M2-M3); c_a(M3-M3); and c_a(M3 top). In general, the sum of c_a(M2 top) and c_a(M3 bottom) is not

equal to c_a(M2-M3), so one has inequality (4). When the design of a metal finger capacitor is such that there is no via between M2 and M3, the sum of c_a(M2 top) and c_a(M3 bottom) is larger than c_a(M2-M3).

We next explain equality (3). Similar to the capacitance density c_a(M2+M3), the capacitance density c_a(M1+M2) for a capacitor consisting of M1 and M2 two levels also contains five components: c_a(M1 bottom), c_a(M1-M1), c_a(M1-M2), c_a(M2-M2), and c_a(M2 top). The capacitance density c_a(M1+M2+M3) for a capacitor made of M1, M2, and M3 three levels contains seven components (Fig. 2): c_a(M1 bottom), c_a(M1-M1), c_a(M1-M2), c_a(M2-M2), c_a(M2-M3), c_a(M3-M3), and c_a(M3 top). Thus, one can see that Eq. (3) holds. The relation (3) for capacitance density can be extended to other level combinations and also be generalized to total capacitance. Namely, to a high degree of accuracy, there exist many capacitance relations (for the same L, W),

$$C(\mathrm{M1}+\mathrm{M2}+\mathrm{M3})+C(\mathrm{M2}) = C(\mathrm{M1}+\mathrm{M2})+C(\mathrm{M2}+\mathrm{M3}), \quad (5a)$$

$$C(\mathrm{M6}+\mathrm{M7}+\mathrm{M8})+C(\mathrm{M7}) = C(\mathrm{M6}+\mathrm{M7})+C(\mathrm{M7}+\mathrm{M8}); \quad (5b)$$

$$C(\mathrm{M1}+\mathrm{M2}+\mathrm{M3}+\mathrm{M4})+C(\mathrm{M2}+\mathrm{M3}) = C(\mathrm{M1}+\mathrm{M2}+\mathrm{M3})+C(\mathrm{M2}+\mathrm{M3}+\mathrm{M4}), \quad (6a)$$

$$C(\mathrm{M2}+\mathrm{M3}+\mathrm{M4}+\mathrm{M5})+C(\mathrm{M3}+\mathrm{M4}) = C(\mathrm{M2}+\mathrm{M3}+\mathrm{M4})+C(\mathrm{M3}+\mathrm{M4}+\mathrm{M5}); \quad (6b)$$

$$C(\mathrm{M1}+\mathrm{M2}+\mathrm{M3}+\mathrm{M4}+\mathrm{M5})+C(\mathrm{M2}+\mathrm{M3}+\mathrm{M4}) = C(\mathrm{M1}+\mathrm{M2}+\mathrm{M3}+\mathrm{M4})+C(\mathrm{M2}+\mathrm{M3}+\mathrm{M4}+\mathrm{M5}), \quad (7a)$$

$$C(\mathrm{M3}+\mathrm{M4}+\mathrm{M5}+\mathrm{M6}+\mathrm{M7})+C(\mathrm{M4}+\mathrm{M5}+\mathrm{M6}) = C(\mathrm{M3}+\mathrm{M4}+\mathrm{M5}+\mathrm{M6})+C(\mathrm{M4}+\mathrm{M5}+\mathrm{M6}+\mathrm{M7}); \quad (7b)$$

$$C(\mathrm{M1}+\mathrm{M2}+\mathbf{L}+\mathrm{M8})+C(\mathrm{M2}+\mathrm{M3}+\mathbf{L}+\mathrm{M7}) = C(\mathrm{M1}+\mathrm{M2}+\mathbf{L}+\mathrm{M7})+C(\mathrm{M2}+\mathrm{M3}+\mathbf{L}+\mathrm{M8}). \quad (8)$$

In each equation, there are capacitance values for four capacitors, and those four capacitors occupy 2x2 adjacent cells in Table 1 for allowed level combinations of metal finger capacitors in a semiconductor technology.

4 SMARTER LEVEL COMBINATION SELECTION

If a semiconductor technology uses three thin metal levels (M1, M2, M3), two 1.3x fat levels (M4, and M5), and three 2x fat metal levels (M6, M7, M8), then there are $K = 8$ metal levels which a metal finger capacitor can use. Thus, there are $8 + 7 + \ldots + 1 = 36$ level combinations, or $K(K + 1)/2$ level combinations for the capacitor. Completely covering all 36 or $K(K + 1)/2$ level combinations in a semiconductor technology testsite would use a lot of silicon area. Generally, a subset of level combinations is chosen. Unfortunately, a set of arbitrarily chosen level combinations often can not reliably project capacitance values for all level combinations. If relation (4) were true, one would be able to use a set of K level combinations in a technology testsite to cover all $K(K + 1)/2$ level combinations. We show that, with a careful selection, a set of only $(2K - 1)$ level combinations can reliably project capacitance values for all $K(K + 1)/2$ level combinations, especially for capacitance characterization. One set of choices is K single-level cases: (M1), (M2), (M3), ..., (M(K–1)), (MK), plus $(K - 1)$ two-level cases (M1 + M2), (M2+M3), (M3+M4), ..., (M(K–2) +M(K–1)), (M(K–1) +MK). These $(2K - 1)$ level combinations are indicated as bold face numbers 1 and 2 in Table 2. After obtaining the capacitance values of K single-level capacitors and of $(K - 1)$ two-level capacitors, one can deduce the capacitance value of $(K - 2)$ three-level metal finger capacitors using Eqs. (5a), (5b), etc. (step a in Table 2). After obtaining the capacitance values of $(K - 2)$ three-level metal finger capacitors, we next find the capacitance value of $(K - 3)$ four-level metal finger capacitors using Eqs. (6a), (6b), etc. (step b in Table 2). After obtaining the capacitance values of $(K - 3)$ four-level metal finger capacitors, one further obtain the capacitance value of $(K - 4)$ five-level metal finger capacitors using Eqs. (7a), (7b), etc. (step c in Table 2). Proceeding in this sequence, at the last step, we get the capacitance of all-level capacitor using relation (8) (step f in Table 2). Another set of $(2K - 1)$ level combinations uses K level combinations that contain the bottom metal level M1, (M1), (M1 + M2), (M1 + M2 + M3), (M1 + M2 + M3 + M4), ..., (M1+ M2 + M3+…+ M(K-1)), (M1 + M2 + M3 +… + M(K-1) + MK), and another $(K - 1)$ level combinations that contain the top-most metal level MK allowed in a metal finger capacitor, (M2 + M3 + … + M(K-1) + MK), (M3 + … + M(K-1) + MK), ..., (M(K-1) + MK), (MK). These $(2K - 1)$ level combinations are indicated as bold face numbers in Table 3. The sequence of obtaining the capacitance values of other level combinations goes like this: First using relation (8) one deduces C(M2 +M3 +… +M(K-1)) (step a in Table 3). Next, we obtain C(M2 +M3 +… +M(K - 2)) and C(M3 +M4 + … +M(K -1)), separately (step b in Table 3). Proceeding in this way, last, one gets the capacitance values of the rest single-level capacitors, C(M2), …, C(M(K–1)) (step f in Table 3). Since measuring the capacitance value of a capacitor reliably in a lab requires a minimum amount of capacitance, this second set has an advantage of having larger capacitance densities and thus needing a smaller wafer area.

Using a level table like Tables 2 and 3, it is easy to construct several other sets of $(2K - 1)$ level combinations, each of which can be used to reliably project capacitance values for all level combinations. For example, a 3rd set of $(2K - 1)$ level combinations consists of K single-level cases (diagonal cells) and other $(K - 1)$ level combinations having top level MK (1st column). A 4th set of $(2K - 1)$ level combinations comprises K single-level cases and other $(K - 1)$ level combinations having bottom level M1.

5 CAPACITANCE MODELING

We include various capacitance components (Fig. 2) in our predictive compact models for metal finger capacitors. The main capacitance of a metal finger capacitor is modeled as

$$C = \sum_{j=1}^{J} [(n_{f,j} - 1)(c_{a,j} l + 2c_{w,j}) + 2c_{l,j} l + c_{0,j}], \quad (9)$$

with

$$c_{a,1} = c_1^{(bot)} + c_1^{(metal)} + \tfrac{1}{2} c_{1,2}^{(via)},$$

$$c_{a,j} = \tfrac{1}{2} c_{j-1,j}^{(via)} + c_j^{(metal)} + \tfrac{1}{2} c_{j,j+1}^{(via)}, \quad j = 2, 3, \mathbf{L}, J-1,$$

$$c_{a,J} = \tfrac{1}{2} c_{J-1,J}^{(via)} + c_J^{(metal)} + c_J^{(top)}, \quad (10)$$

where n_f is the number of fingers, and l is the common finger length. Notice that the value of $c_1^{(bot)}$ varies with whether j = 1 level is M1, M2, or M3, etc., and the value of $c_J^{(top)}$ also depends on whether the via above $j = J$ level is a 1x via, a 1.3x via, or a 2x via, etc. Similarly, the value of capacitance in a via space, $c_{j,j+1}^{(via)}$, varies with whether the via between the j^{th} and $(j + 1)^{th}$ metal levels is a 1x via, a 1x-1.3x transitional via, a 1.3x via, a 1.3x-2x transitional via, or a 2x via. When there is no via between a finger and finger above it (e.g., typically there is no via on fingers for a transitional via level; call them Mx and My levels in the following), there exist some inequality relations. For example,

$$C(\mathrm{Mx} + \mathrm{My}) < C(\mathrm{Mx}) + C(\mathrm{My}). \quad (11)$$

There is also parasitic capacitance between the bottom finger face of a capacitor and substrate and between the side walls of most outside fingers and substrate. We also include these parasitic capacitance components in our compact model for metal finger capacitors.

6 RESISTANCE MODELING

For a metal finger capacitor using only one metal level, the total resistance of a metal finger capacitor consists of resistance in metal fingers and resistance in two tabs,

$$R_{tot} = R_{fingers} + 2R_{tab}, \quad (12)$$

with

$$R_{fingers} = 4(\tfrac{1}{3} l + s_{tip}) r(w_f) / n_f, \quad (13a)$$

$$R_{tab} = \tfrac{1}{12} r_k(w_{tab}) W, \quad (13b)$$

where s_{tip} is the space between a finger tip and the tab, and $r(w)$ is resistance per unit length for a wire of width w at the given metal level. Note that $l + 2(w_{tab} + s_{tip}) = L$. For a square shape capacitor (say, $l + 3s_{tip} = W$), the finger part of resistance becomes smaller than the tab part of resistance when the size of the capacitor increases,

$$\frac{R_{fingers}}{R_{tab}} = \frac{16 r(w_f)}{n_f r(w_{tab})} = \frac{16 p r(w_f)}{W r(w_{tab})},$$

where p is the finger pitch (i.e., the sum of finger width w_f and finger space). For example, when tab width w_{tab} is large compared to finger width w_f such that

$$r(w_f) = 10 r(w_{tab}) \quad (14)$$

and when p = 0.02 μm (in a 65 nm technology without vias on fingers or in a 45 nm technology with vias on fingers), finger resistance equals one-tab resistance, $R_{fingers} = R_{tab}$ when W = 32 μm, but $R_{fingers} = R_{tab}/5$ when W = 160 μm. A square shape capacitor may not be an optimal choice. We next show how to maximize the quality factor

$$Q = \frac{\mathrm{Im}\, Y_{11}}{\mathrm{Re}\, Y_{11}} \approx \frac{1}{2pf R_{tot} C} \quad (15)$$

of a capacitor under a constraint of a fixed total capacitance C, where f is the frequency of a signal. This problem is equivalent to minimize the total resistance R_{tot} at a fixed total capacitance C. To the first order, this means to minimize the total resistance R_{tot} at a fixed total finger length,

$$l_{tot} = n_f l. \quad (16)$$

Using $W = n_f p$ and $l >> 3s_{tip}$, the total resistance can be re-written as

$$R_{tot} \approx \frac{4 l_{tot} r(w_f)}{3 n_f^2} + \frac{1}{6} r(w_{tab}) n_f p \equiv \frac{b}{n_f^2} + 2a n_n.$$

The total resistance R_{tot} is minimized when the finger resistance equals one-tab resistance, at which the finger number is found to be

$$n_f = \mathrm{int}\left(\sqrt[3]{\frac{b}{a}} + 0.5 \right) = \mathrm{int}\left(\sqrt[3]{\frac{16 l_{tot} r(w_f)}{p r(w_{tab})}} + 0.5 \right), \quad (17)$$

and the corresponding common finger length follows from Eqs. (16) and (17) as

$$l = \frac{l_{tot}}{\mathrm{int}\left(\sqrt[3]{b/a} + 0.5 \right)}. \quad (18)$$

The corresponding value of the ratio l/W is

$$\frac{l}{W} = \frac{l_{tot}}{p[\mathrm{int}\left(\sqrt[3]{b/a} + 0.5 \right)]^2},$$

which is closely related to the capacitor's aspect ratio L/W. For example, under condition (14) and when the total finger length l_{tot} is 10,000 times of finger pitch p, $l_{tot} = 10{,}000p$, Eqs. (17) and (18) give $W/p = n_f = 117$, $l = 85p$, and the ratio $l / W = 0.73$, i.e., the common finger length l is smaller than capacitor width W. Figure 3 plots the device size ratio l/W as a function of total finger length l_{tot} for several values of the ratio $r(w_f)/r(w_{tab})$ of two unit-length resistances.

For a metal finger capacitor comprising multiple metal levels (without via on fingers), its total resistance contains the contributions from the resistance in each of multiple metal levels (described above) and from the resistance of vias connecting tabs in multiple metal levels.

7 SUMMARY

We have presented a method to systematically characterize and model the capacitance and resistance properties of multi-level metal finger capacitors. We revealed capacitance relations among capacitors consisting of different metal levels and also presented many modeling results for the first time.

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REFERENCES

[1] J. Kim *et al.*, *VLSI Symp. Circuits Dig.*, 2003, pp. 29–32.

[2] D. Kim *et al.*, *IEEE Electron Device Lett.*, vol. 28, 2007, pp. 616–618.

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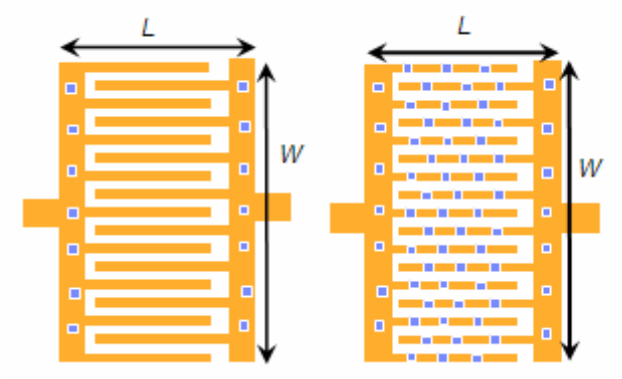

Fig. 1. Layout views of metal finger capacitors. Left: no via on fingers. Right: with vias on fingers.

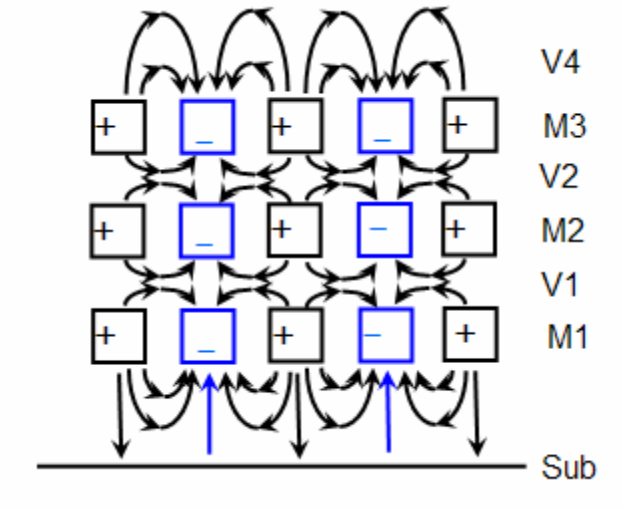

Fig. 2. A cross-section view of a finger capacitor. Electric field lines in via space, above the top metal level, and below the bottom metal level are also shown schematically.

Bot\Top	M8	M7	M6	M5	M4	M3	M2	M1
M8	X							
M7	(5b)	(5b)						
M6	(5b)	(5b)	X					
M5	X	X	X	X				
M4	X	(7b)	(7b)	X	X			
M3	X	(7b)	(7b)	(6b)	(6b)	X		
M2	(8)	(8)	X	(6b)	(6b)	(5a)	(5a)	
M1	(8)	(8)	X	X	X	(5a)	(5a)	X

Table 1. Four capacitors whose capacitance values appear in each of Eqs. (5a), (5b), (6b), (7b), and (8) occupy 2x2 adjacent cells in a table for allowed level combinations. Letter X indicates the rest of allowed level combinations.

Bot\Top	M8	M7	M6	M5	M4	M3	M2	M1
M8	**1**							
M7	**2**	**1**						
M6	a. 3	**2**	**1**					
M5	b. 4	a. 3	**2**	**1**				
M4	c. 5	b. 4	a. 3	**2**	**1**			
M3	d. 6	c. 5	b. 4	a. 3	**2**	**1**		
M2	e. 7	d. 6	c. 5	b. 4	a. 3	**2**	**1**	
M1	f. 8	e. 7	d. 6	c. 5	b. 4	a. 3	**2**	**1**

Table 2. A set of $(2K - 1)$ level combinations (shown by bold letters) for $K = 8$. A number indicates the number of metal levels. Letters a, b, c, …, f label the steps of deducing capacitance values of other level combinations.

Bot\Top	M8	M7	M6	M5	M4	M3	M2	M1
M8	**1**							
M7	**2**	f. 1						
M6	**3**	e. 2	f. 1					
M5	**4**	d. 3	e. 2	f. 1				
M4	**5**	c. 4	d. 3	e. 2	f. 1			
M3	**6**	b. 5	c. 4	d. 3	e. 2	f. 1		
M2	**7**	a. 6	b. 5	c. 4	d. 3	e. 2	f. 1	
M1	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**

Table 3. Another set of $(2K - 1)$ level combinations (shown by bold letters) for $K = 8$. Letters a, b, c, …, f label the steps of deducing capacitance values of other level combinations.

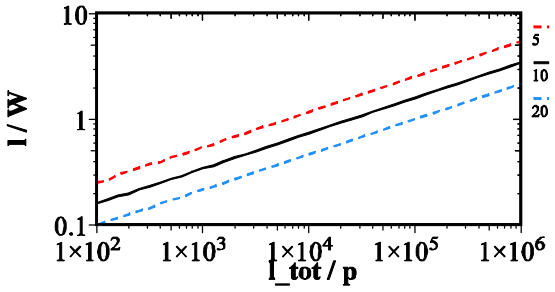

Fig. 3. The ratio l/W (that minimizes the resistance of a single-level capacitor) as a function of l_{tot} for several values of the ratio $r(w_f)/r(w_{tab})$ of two unit-length resistances.