UF "Compact" Models: A Historical Perspective

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ABSTRACT

The history of the developments of "compact" models for SOI MOSFETs at the University of Florida (UF) is reviewed. The uniqueness and innovation of the UF "process-based" models are reiterated, and their global utility as excellent SOI research/education tools for more than 25 years is exemplified. Floating-body (FB) hysteresis, G-S/D underlap, bulk inversion, and pseudo-latch (recent) are noted as new insights on SOI devices (i.e., PD and FD MOSFETs, DG FinFETs, and FB DRAM cells) that were attained using the UF "ugly duckling" Spice compact models.

Keywords: SOI MOSFETs, DG MOSFETs, SOISPICE, UFSOI, UFPDB, UFDG

1. HISTORY OF MODEL DEVELOPMENTS

In 1982 we began developing what we called "process-based" compact models for SOI MOSFETs, so called because the key model parameters relate directly to the device structure, defined by the device processing, as well as to the underlying physics. The model cards for these UF models can hence be estimated very quickly, and then fine-tuned based on limited measured device data. Thus, the models, implemented in a circuit simulator, are quasi-predictive, and are useful for device/technology design as well as circuit design. Indeed, the UF models are, in essence, compact device simulators with extraordinary computational efficiency. This is why they have been thought of as "ugly duckling" Spice compact models. They have, however, served as excellent SOI research/education tools around the world for more than 25 years.

I stress that our UF models have always been "surface potential-based," which is thus a 29-year-old compact-model concept. Such a basis is essential for truly physical compact modeling of MOSFETs. Further, our models have always been "charge-based," as opposed to capacitance-based, to ensure charge conservation, which is especially important in floating-body SOI MOSFETs. This physical charge basis of our 'NFD' (non-fully depleted) model [1] in 'SOISPICE' [2] enabled prediction of "hysteresis" (a.k.a. history effect) in PD (partially depleted)/SOI MOSFETs in 1994 [3]. The NFD and 'FD' (fully depleted) [4] models in SOISPICE (a version of Spice2), which were first released in 1988, were continually upgraded, evolving to the 'UFSOI' models [5] (in Spice3) in 1997.

In 2000 the UFSOI/NFD model was expanded to become 'UFPDB' [5], [6], a unified model for PD/SOI and bulk-Si MOSFETs. The network representation of the five-terminal UFPDB model (gate-tunneling current is included, but not depicted) is shown in Fig. 1. The current and charge modeling, for the parasitic BJT as well as the intrinsic MOSFET, is physically coupled. The model formalisms, involving Newton-like iterative solutions of physics-based nonlinear equations, include accountings for all important nanoscale-device mechanisms, e.g., carrier energy quantization and carrier velocity saturation with possible overshoot.

In 2001 the UFSOI/FD model was upgraded and refined to become 'UFDG' [7]-[10] (in Spice3 for Unix and in Ngspice for Linux), a generic double-gate (DG) MOSFET model applicable to nanoscale FinFETs and single-gate (SG) FD/SOI MOSFETs with ultra-thin bodies (UTBs). Its network representation is similar to that of UFPDB in Fig. 1, and its model formalisms are similarly physical. Its Poisson-equation solution for the front and back surface potentials is, however, quite different, being rigorously 2-D in weak inversion and accounting for arbitrarily asymmetrical gate structures (i.e., boundary conditions) while iteratively and self-consistently incorporating the Schrödinger equation for the quantization effects. UFDG, which is currently being licensed by the University of Florida, is still being upgraded as needed today.

2. CHRONICLE OF NEW INSIGHTS ATTAINED WITH THE MODELS

2.1. Hysteresis

Floating-body effects are especially apparent in PD/SOI MOSFETs (and in FD/SOI devices with back-surface

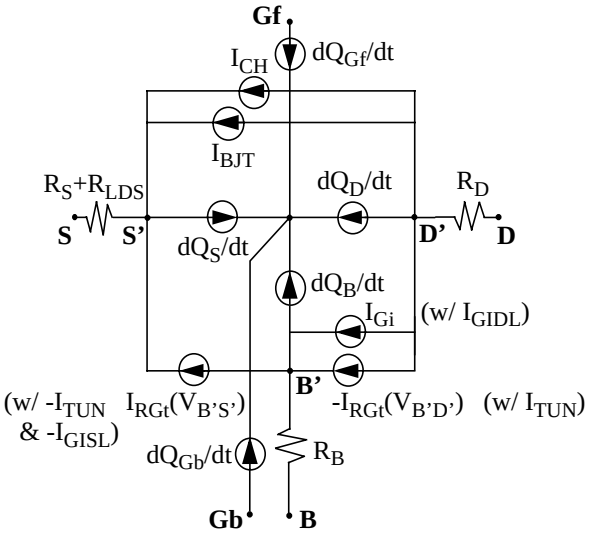


Fig. 1 [6]. Network representation of the UFPDB model.

accumulation) where they result from the dependence of threshold voltage (V_t) on the body voltage (V_{BS}), which is defined by the charge condition of the body. In general, V_{BS} is dynamic, being defined by the FB nodal equation,

$$I_G - I_R = \frac{dQ_B}{dt}\ , \qquad (1)$$

where Q_B is the body charge (that is supported by the body terminal), which is linked to the other terminal charges via neutrality as indicated in Fig. 1, and I_G and I_R represent all the carrier generation and recombination currents linked to the body as shown in Fig. 1. All the terms in (1) can depend on V_{BS}, which can be positive or negative, and hence the physics underlying the FB effects, both DC and transient, can be quite complex. The evolution of PD/SOI CMOS technology has depended on good understanding and control of these effects.

In the early 1990's, we were using our NFD model in SOISPICE to study the FB effects, especially the transient ones which were most complex. We were monitoring V_{BS} and V_t in transient simulations of PD/SOI inverter circuits, and discovered an anomalous hysteretic variation in V_t [3]. We initially thought that the SOISPICE predictions, exemplified in Figs. 2 and 3, were resulting from numerical error; no one suspected such a floating-body effect 20 years ago. Now, it is known to be pervasive in SOI CMOS. For example, propagation delays are hysteretic as shown by UFSOI/NFD simulations in Fig. 4 [11], and must be addressed via conservative margin design and/or advanced device design to suppress FB effects. Further, the hysteresis, which is generally due to relatively slow R/G transients superimposed on fast switching transients, is the basis of FB DRAM cells [12].

2.2. G-S/D Underlap

As CMOS is being scaled toward <10nm gate lengths, new nonclassical devices are necessarily being considered, mainly because random doping-fluctuation effects limit the scalability of classical devices. The primary nonclassical devices being considered are the DG FinFET and the planar FD/SOI MOSFET with thin BOX, both of which have undoped UTBs/channels. Such devices can have unusual features, as we have discovered with our models.

UFDG has revealed some surprising features of DG MOSFETs. For example, in 2003, when calibrating UFDG to DG FinFETs fabricated at AMD, we discovered that the effective channel length (L_{eff}) of undoped-UTB devices tends to be longer than the gate length (L_g), and bias-dependent as well, due to "G-S/D underlap" [13]. The partial calibration results in Fig. 5, for an L_g = 17.5nm nFinFET, clearly revealed this new insight, unbeknown to AMD and everyone else. Such underlap is beneficial to the control of short-channel effects (SCEs) and I_{off}, as indicated by the measured SCEs versus L_g in Fig. 6 [13] where, as we found, L_{eff} is (too) much longer than L_g. We also found, however, that there is a design tradeoff involving S-D series resistance

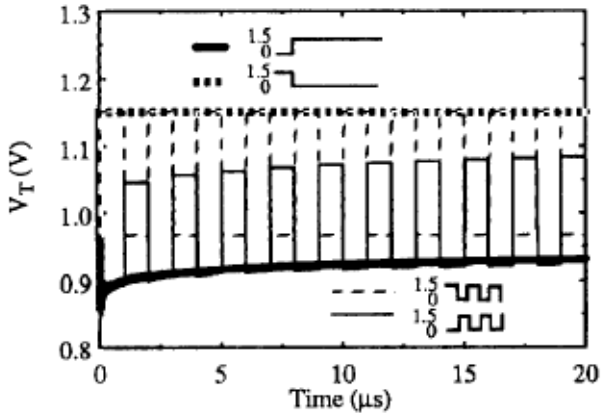


Fig. 2 [3]. SOISPICE-predicted transient threshold voltage of a FB PD/SOI MOSFET (L_g = 0.2μm) corresponding to gate-voltage pulses having different initial values and frequencies. The different bias conditions result in different $V_t(t)$, or V_t hysteresis.

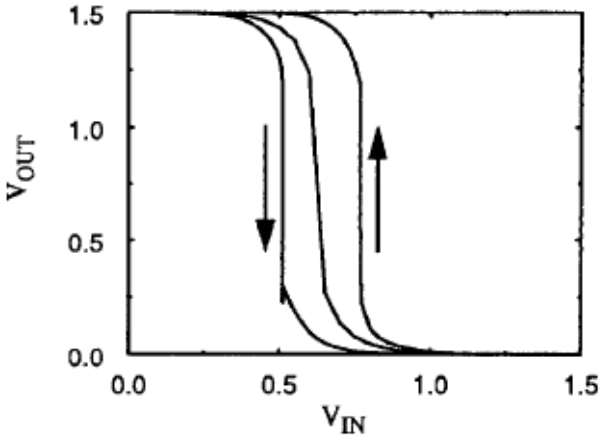


Fig. 3 [3]. SOISPICE-simulated forward- and reverse-swept slow-transient voltage-transfer characteristics of a FB PD/SOI CMOS inverter. Comparison with the DC transfer curve, also shown, reveals the V_t hysteresis in the device being switched from off to on.

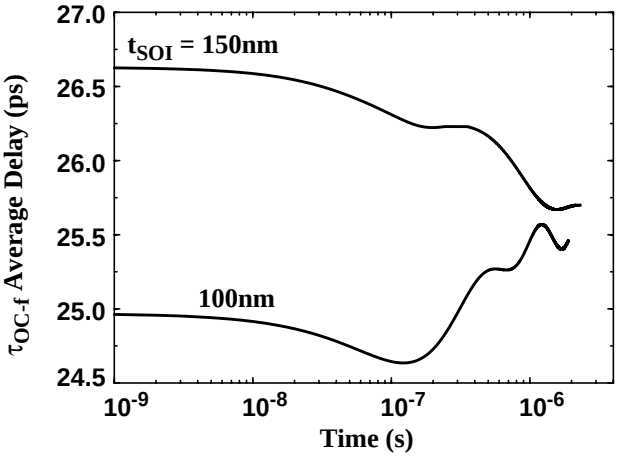


Fig. 4 [11]. UFSOI/NFD-predicted open-chain PD/SOI CMOS (L_{eff} = 145nm) inverter delay for two SOI thicknesses, showing how the drain-body capacitance, dependent on the SOI thickness, affects the hysteretic delay.

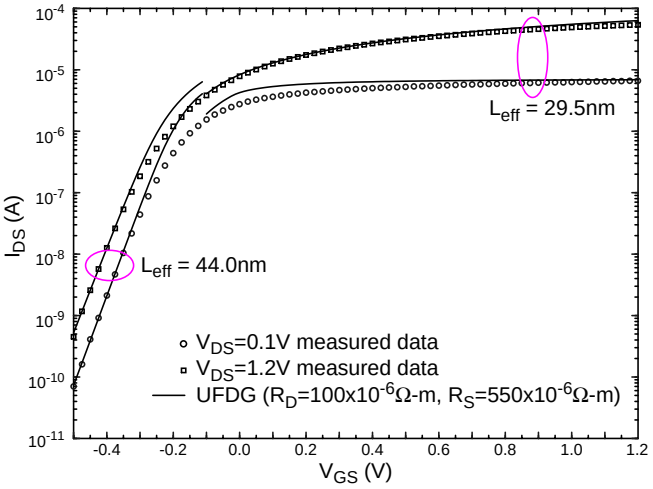


Fig. 5 [13]. Partial UFDG calibration to an L_g = 17.5nm nFinFET; t_{Si} = 17nm. With L_{eff} = L_g + 26.5nm (≅13nm G-S/D underlap), the measured weak-inversion I_{DS}-V_{GS} characteristics are predicted well; with shorter L_{eff} = L_g + 12.0nm (~2L_{Debye}), the strong-inversion curves are predicted reasonably well. The underlap, heretofore unknown, and its bias dependence are clearly implied. The high source resistance noted for the UFDG calibration means that the underlap here is much too long. (UFDG now accounts for a V_{GS}-dependent L_{eff}.)

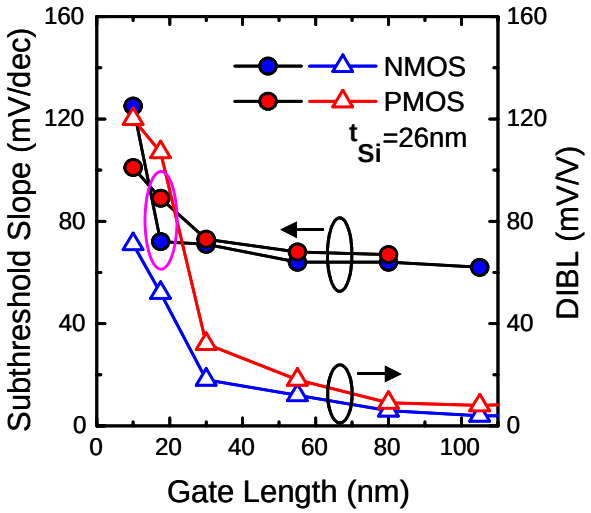


Fig. 6 [13]. Measured SCEs vs. L_g of CMOS DG FinFETs. The outstanding control of DIBL and S in the nanoscale devices is due to G-S/D underlap and L_{eff} > L_g in weak inversion. For example, the encircled data are for the L_g = 17.5nm device of Fig. 5 for which L_{eff} = 44nm.

and I_{on}, as alluded to in Fig. 5. Indeed, G-S/D underlap has become an essential part of nanoscale FinFET design, and of SG FD/SOI MOSFET design as well [14], and compact models must account for the anomalies it produces, e.g., the bias-dependent L_{eff}.

2.3. Bulk Inversion

Further, UFDG, with its physical modeling of quantization that renders it a "compact Poisson-Schrödinger solver," has given new insights on channel current, or I_{on}, in these nonclassical nanoscale CMOS devices with undoped bodies. For example, it shows, when compared with UFPDB simulations and measurements of classical, doped-channel MOSFETs, how "bulk inversion" decreases the current due to lowered strong inversion-layer capacitance (C_i), even when the quantization effect (which further lowers C_i) is not accounted for. This is the main reason why current in a DG FinFET always tends to be less than twice that in a classical SG counterpart (in which C_i is higher due to the higher transverse electric field).

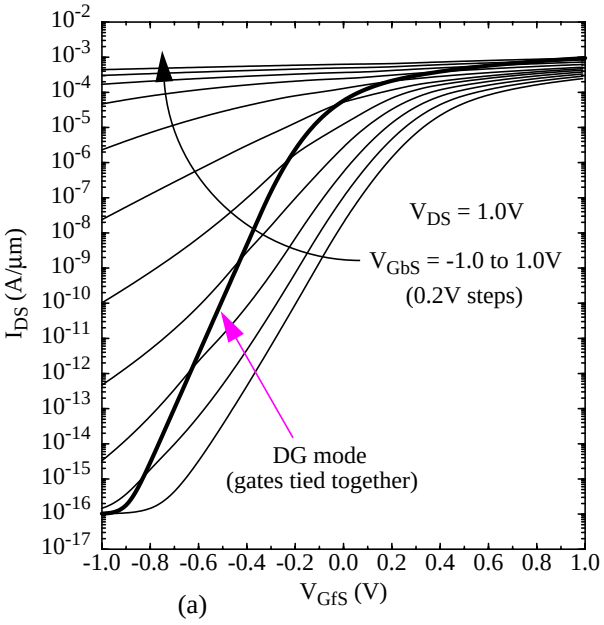
The UFDG simulation results for an L_g ≅ 80nm DG nFinFET shown in Fig. 7 with experimental corroboration [15], including the independent-gate mode (MIGFET) which UFDG allows, reflect this detrimental effect of bulk inversion. Note, even with n^+-polysilicon gates which yield V_t < 0, I_{on} of the FinFET is only about 1mA/μm, which is actually less than the typical current achieved in classical SG counterparts. Heretofore, bulk (a.k.a. volume) inversion, which, indeed, prevails in strong inversion as shown in Fig. 8 [16], was thought to be beneficial (because of higher carrier mobility). The bulk inversion further renders the effective width of a triple-gate (TG) FinFET undefinable simply in terms of the gate area [16], as implied in Fig. 8.

2.4. Pseudo-Latch

There is much interest today in lowering the operating voltage (V_{DD}) of nanoscale CMOS to reduce power consumption. The Maxwell-Boltzmann 60mV/decade limit of the MOSFET subthreshold slope (S), however, precludes an acceptable I_{on}/I_{off} ratio for V_{DD} much less than 1V. So, there is interest now in novel FETs that can yield S < 60mV/decade in a viable CMOS technology.

We recently reported an anomalous floating-body effect in SOI MOSFETs that could make them candidates for such application [17]. Measured and numerically simulated I_{DS}-V_{GS} characteristics of nanoscale FD/SOI devices, biased for accumulation at one surface of the SOI body to enable FB effects, showed, for particular device structures (e.g., thick t_{ox}), a subthreshold latch mechanism by which the current increased abruptly with extremely low S. This mechanism is not fully understood, and has been attributed by some to a breakdown of the parasitic BJT, even though V_{DS} was less than BV_{CEO} in [17].

We used UFPDB to analyze this anomalous FB effect. We first assumed a PD/SOI nMOSFET representative of the L_g = 60nm node (t_{ox} = 2nm, n^+-polysilicon gate, retrograded channel doping profile), but without processing to limit the FB effects [e.g., to enhance I_R and limit V_{BS} in (1)]. The predicted DC current-voltage characteristics plotted in Fig. 9 clearly show the FB enhancement of I_{off} at high V_{DS} resulting from V_t lowering by V_{BS} > 0 due to impact ionization-current [I_{Gi} ≅ I_G) charging of the body [18]. However, note in Fig. 9 what happens when t_{ox} is increased. For very thick t_{ox} = 12nm, UFPDB predicts a subthreshold "pseudo-latch" with an infinitesimally low S at high V_{DS}.



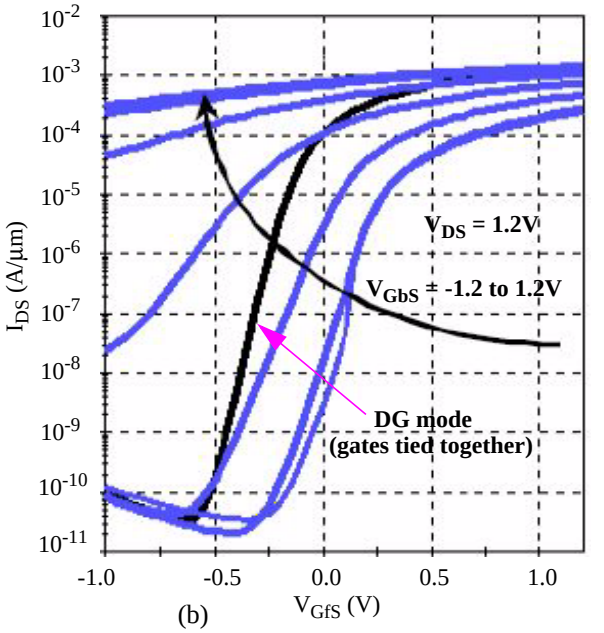


Fig. 7 [15]. (a) UFDG-predicted current-voltage characteristics (per h_{Si}) of an undoped L_g = 80nm n-channel DG FinFET; t_{Si} = 25nm, t_{oxf} = t_{oxb} = 2.0nm. (b) Measured current-voltage characteristics (per h_{Si}) of an undoped L_g =70nm DG FinFET, the structure (t_{Si} = 25nm, t_{oxf} = t_{oxb} = 2.4nm) of which is comparable to that of (a). The MIGFET-mode characteristics, for varying back-gate bias, are also shown. The DG-mode on-state currents reflect degradation due to bulk inversion.

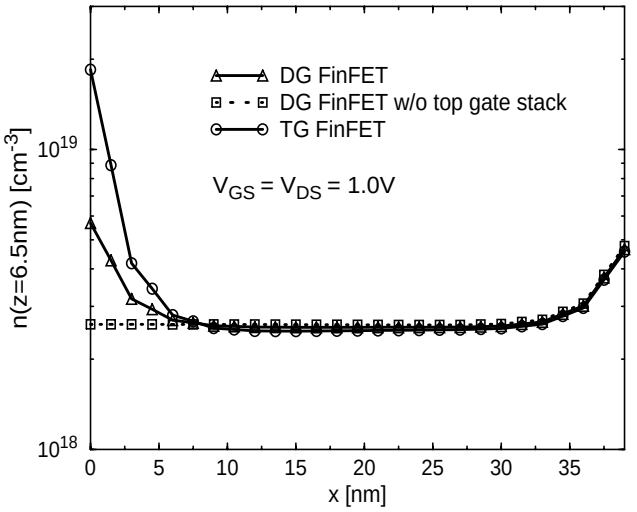


Fig. 8 [16]. 3-D Davinci-predicted on-state electron density down the middle of the fin, at the center of the channel (y = L_g/2), in nanoscale, undoped DG and TG nFinFETs; L_{eff} = 25nm, t_{Si} = 13nm, h_{Si} = 39nm, t_{ox} = 1.2nm, t_{BOX} = 200nm, and midgap metal gates. The bulk-inversion charge is predominant in the on-state condition.

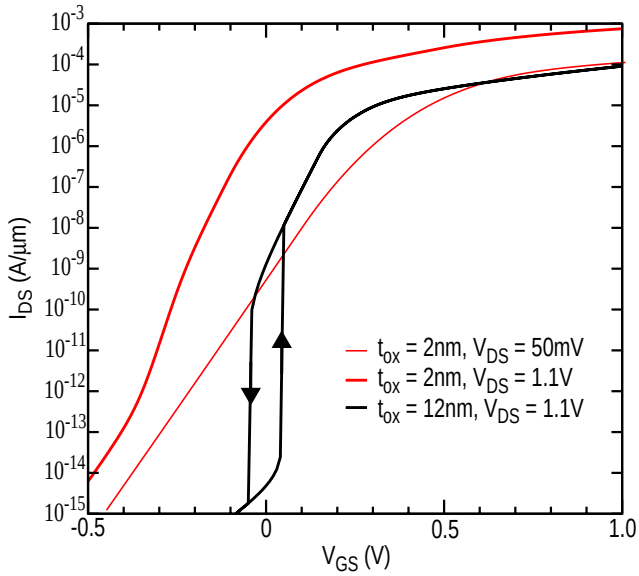


Fig. 9. UFPDB-predicted DC current-voltage characteristics of an L_g = 60nm PD/SOI MOSFET for nominally thin and abnormally thick gate-oxide thicknesses. For the thin-t_{ox} device, the low-V_{DS} curve indicates $V_t \cong$ 0.3V, and the high-V_{DS} curve reflects significant V_t lowering due to the usual FB effect [18]. For the thick-t_{ox} device, the high-V_{DS} curves show an abrupt subthreshold pseudo-latch, as observed in [17], with hysteresis as indicated by the forward- and reverse-V_{GS} sweeps. The BJT option in UFPDB was turned off for all simulations, as was GIDL current to facilitate explanation of the pseudo-latch effect.

This latch is not associated with the parasitic BJT; we had the BJT option in UFPDB turned off for all the simulations of Fig. 9.

Our process-based UFPDB gives us physical insight needed to explain this anomalous pseudo-latch. We find that at the latch bias (V_{GS} ~ 0V in this example), dV_{BS}/dV_{GS} is extremely large due to very strong positive feedback in the $I_{ch}(V_{GS}, V_{BS})$ - $I_{Gi}(I_{ch})$ - $I_R(V_{BS})$ loop. With this insight, we can use analytic descriptions of the three noted currents in this loop, with the DC form of (1), and derive, for weak inversion,

$$\frac{dV_{BS}}{dV_{GS}} \cong \frac{m}{1-r(m-1)} \qquad (2)$$

where m (generally between 1 and 2, and V_{BS}-dependent) is the nonideality exponential factor in the $I_R(V_{BS})$ expression, and $r = -dV_t/dV_{BS} = C_d/C_{ox} \cong 3t_{ox}/t_d$ is the body-effect factor of the MOSFET; C_d is the depletion capacitance and t_d is the depletion-region thickness, both of which are defined by the channel doping profile. Note in (2) that dV_{BS}/dV_{GS} approaches infinity for $m \rightarrow 1 + 1/r \cong 1 + t_d/(3t_{ox})$, which is reflected by the pseudo-latch in Fig. 9 for the thick-t_{ox} device. The latch subsides as m approaches 1 with V_{BS} increasing abruptly. For thin t_{ox}, the noted latch value of m cannot be approached because of the noted physical constraints on m.

Note also in Fig. 9 the hysteresis defined by the predicted forward- and reverse-V_{GS} sweeps, which must be limited as the pseudo-latch device is designed for acceptable V_t. Indeed, there are many issues in this novel idea that must be addressed, including ones associated with the fast-transient pseudo-latch, or lack thereof. Nonetheless, perhaps it may be possible to design an SOI MOSFET to exploit the pseudo-latch, and achieve a very good I_{on}/I_{off} ratio with very low V_{DD}. And, a model like UFPDB, which can quickly predict sensitivities of the anomalous effect to device parameters such as t_{ox}, t_d, and m, can be invaluable in such design.

3. SUMMARY

The developments of UF process-based "compact" MOSFET models have been reviewed, and exemplary new physical insights on SOI devices attained with the models have been overviewed. Indeed, the UF models have been, and are effective research/education tools. The "ugly duckling" has prevailed, just like in the fairy tale (illustrated in Fig. 10) [19]! (Is this my swan song?)

ACKNOWLEDGMENTS

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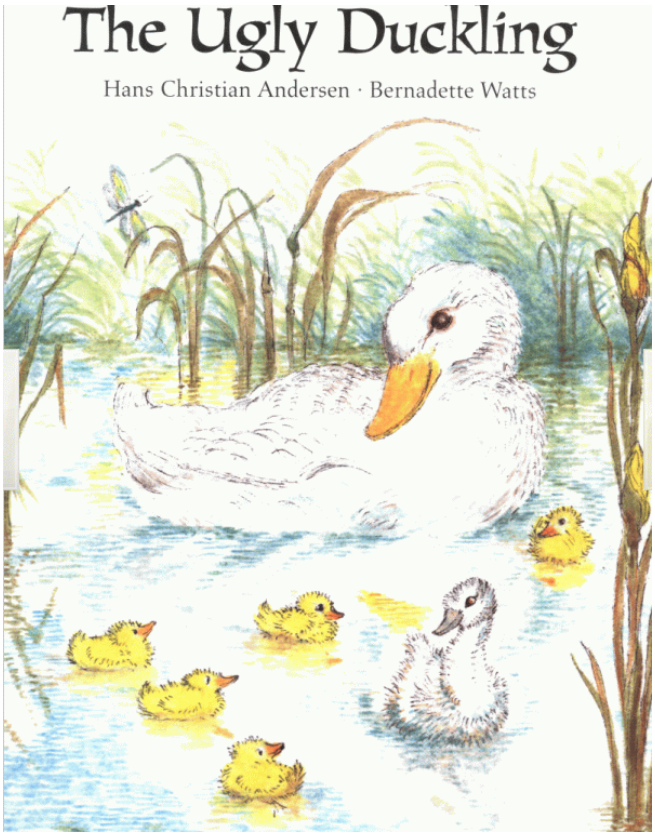

Fig. 10 [19]. The UF-model metaphor.

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