

Impact of Gate-Induced-Drain-Leakage Current Modeling on Circuit Simulations in 45nm SOI Technology and Beyond

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ABSTRACT

In this paper we investigate and analyze the impact of gate-induced-drain-leakage (GIDL) current modeling on silicon-on-insulator (SOI) transistor output characteristics, ON-state floating body potential, switching delay and history in a 45nm partially-depleted SOI (PDSOI) ring oscillator. It was found that GIDL current dominates the junction leakage even at zero gate bias and nominal drain bias of 1.0V. Simulation results from models with different GIDL components but similar OFF-state junction leakage show that different GIDL modeling has a strong impact on the resulting floating body potential and IV characteristics, which affects both history and ring delay time. These results suggest that even for digital circuit simulations in 45nm SOI technologies, GIDL current needs to be accurately included in optimizing the circuit for power and performance.

Keywords: gate-induced-drain-leakage, silicon-on-insulator, floating body effect, history effect

1 INTRODUCTION

Leakage reduction becomes increasingly important for low power applications in the forthcoming generation of MOSFET devices. Besides gate leakage and junction diode leakage, another important leakage source is the gate-induced-drain-leakage (GIDL). The impact of GIDL current reported so far primarily focuses on device characteristics in either the breakdown regime [1] or OFF-state [2], where the voltage drop across the gate-drain overlap region is $> 1.2V$. Therefore, due to the fact that silicon-on-insulator (SOI) technologies are mainly targeted for digital applications and as the power supply voltage scales down to reduce power dissipation in digital circuits, the effect of GIDL current was considered less important compared to gate to source/drain leakage in SOI devices. However, the GIDL current affects the floating body potential in SOI devices and may have bigger impact on circuit simulations than the direct contribution to leakage from GIDL alone.

Recently, the effect of body currents on the hysteresis of short-channel SOI devices was analyzed in [3], with emphasis on the impact ionization current but not the GIDL current. In this paper, we investigate and analyze

the impact of GIDL modeling on the floating body potential for devices in the ON-state and its effect on history and delay results in ring oscillators in 45nm PDSOI technology. It was found that GIDL current dominates the junction leakage even at zero gate bias and nominal drain bias of 1.0V. Simulation results from models with different GIDL components but similar OFF-state junction leakage show significant differences in the resulting floating body potential, IV characteristics, history and ring delay time. These results indicate that when optimizing the digital circuit for power and performance, GIDL current needs to be accurately included in the model during circuit simulations in 45nm PDSOI technologies.

2 DATA COLLECTION

In contrast to the conventional GIDL measurement techniques[1],[2], GIDL current can not be directly measured using current flowing through the drain terminal due to the high gate-to-drain leakage in 45nm SOI. As shown in Fig.1, the drain current is dominated by gate-to-drain leakage in the accumulation region where GIDL current is more significant. The current flowing through the body terminal is a combination of GIDL, diode and gate-to-body leakage currents. In this work, different measurement setups are used to extract the GIDL current and examine its effects, which are shown in Fig.2.

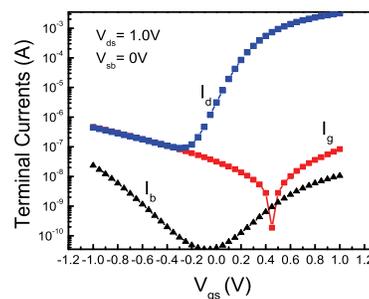
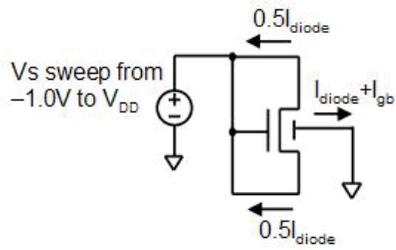
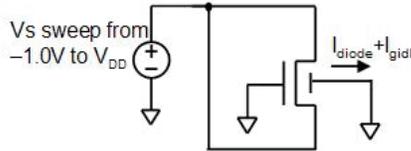


Figure 1: Terminal currents of an SOI MOSFET in 45nm technology.



(a) For diode current collection



(b) For GIDL current collection

Figure 2: Measurement setup for SOI GIDL current extraction

In Fig. 2(a), the drain, source and gate terminals are swept simultaneously from -1.0V to V_{DD} with the body terminal grounded. The current following from the drain/source terminal in this setup is diode current only. In Fig. 2(b), both gate and body terminals are grounded while source and drain terminals are swept from -1.0V to V_{DD} simultaneously. There is a voltage drop between gate and source/drain terminals and GIDL current flows from the drain to the body terminal. The total body current in this case is $I_{diode} + I_{gidl}$. By subtracting the diode current from the total body current data, GIDL current as a function of different terminal biases can be obtained.

With the test setups described above, GIDL current is measured as a function of V_{dg} at different V_{db} (Fig. 3), different temperatures (Fig. 4) and for devices with different effective doping concentration (Fig. 5) respectively.

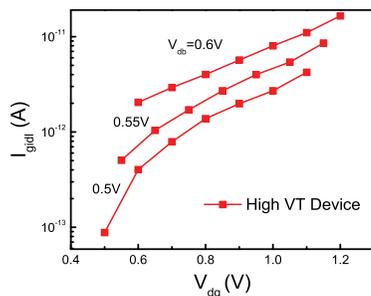


Figure 3: GIDL current a function of V_{dg} at different V_{db} at 25°C in 45nm SOI.

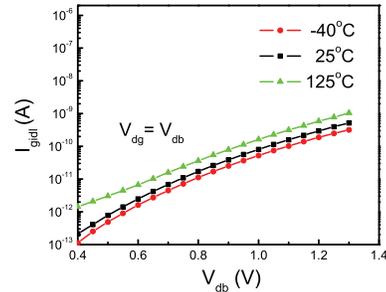


Figure 4: GIDL current as a function of V_{db} with $V_{gs} = 0$ at different temperatures.

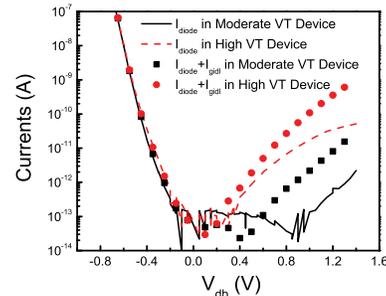


Figure 5: Total body current and GIDL as a function of V_{db} at $V_{gs} = 0$ for devices with different doping concentration at 25°C .

The dependence of GIDL current with respect to V_{dg} in 45nm SOI agrees with the formula given for band-to-band-tunneling (BBT) [4]:

$$I_{BBT} = \frac{A}{B} \cdot W \cdot (E^{max})^2 \cdot \exp\left(-\frac{B}{E^{max}}\right) \quad (1)$$

where A , B and W are predefined coefficients and

$$E^{max} = \frac{\epsilon_{ox}}{\epsilon_{Si}} \cdot \frac{V_{dg} - V_{fb} - \phi_s}{T_{ox}} \quad (2)$$

is the electric field in the gate-drain overlap region. Here ϵ_{ox} and ϵ_{Si} are the dielectric constants of SiO_2 and Si respectively. T_{ox} is the oxide thickness, V_{fb} is the flat-band voltage and ϕ_s is the surface potential at the gate-drain overlap region. Besides the V_{dg} dependence commonly reported, for device with the same doping profile, GIDL current increases with an increase of V_{db} due to the two-dimensional nature of the junction field and the enhanced transport of the electron-hole pairs at high V_{db} . In Fig. 5 when effective channeling doping was increased, the GIDL current increases by almost one order of magnitude. This is expected since as channel charge increases, the drain to body junction becomes more abrupt and the lateral field across the junction becomes stronger, thus GIDL current increases. The

GIDL current data at different temperatures demonstrates a weak but nevertheless positive temperature dependence, which further illustrates that the current is predominately BBT current (Fig. 4).

Note that the results presented here are for a P-type device; for N-type devices in the same technology much less GIDL current is observed.

3 MODEL EXTRACTION

Two models with the same set of parameters except for diode and GIDL models are constructed for a $W = 1.0\mu\text{m}$, $L = 40\text{nm}$ PFET. Both models match to the body current data at zero gate bias with ParamSet1 using only diode current while ParamSet2 using both diode and GIDL currents. As shown in Fig. 6, the two set of parameters provides almost identical results if the drain to body leakage current at zero gate bias is the only concern. However, when the drain-body leakage current at different gate biases is examined, very different results are obtained between two models (Fig. 7). For model with GIDL included, the body current increases with more negative V_{gs} instead of independent of the gate bias. At around $V_{ds} \approx 1.0\text{V}$, the GIDL current becomes significant even at $V_{gs} = 0\text{V}$. The data corresponds to an experimental value of $B \approx 7.5\text{ MV/cm}$, which is much smaller than the theoretical value of $B \approx 21.3\text{ MV/cm}$ [5]. This could be due to the lower bandgap in the high SiGe embedded source/drain regions.

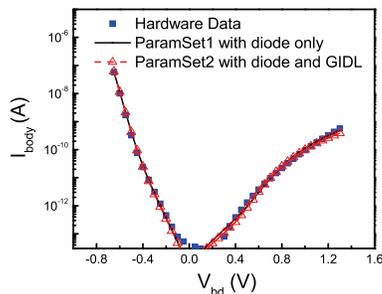


Figure 6: Two different parameter sets give the same source/drain-to-body leakage current at zero gate bias.

To illustrate the effect of different GIDL components on the device characteristics in the ON-state, the output currents as a function of drain and gate biases are plotted for both models (Fig. 8 and Fig. 9). The drain current bias dependence are similar between models with different GIDL components at high gate biases since GIDL is much less at strong inversion region. At low gate biases, as shown in Fig. 8 and Fig. 9, model with GIDL shows a higher subthreshold current due to the larger floating body potential caused by strong GIDL

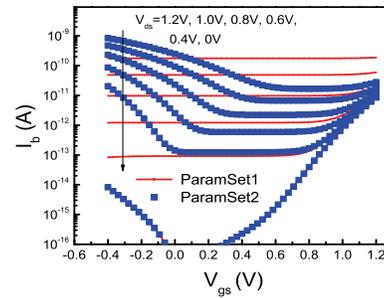


Figure 7: The simulated body currents using ParamSet1 and ParamSet2.

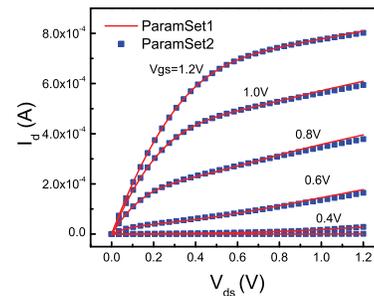


Figure 8: The drain current as a function of drain biases.

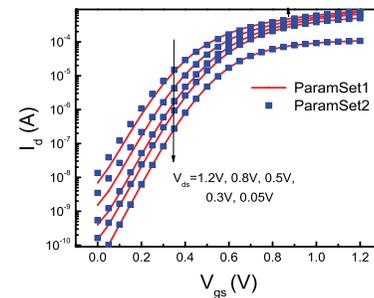


Figure 9: The drain current as a function of gate biases.

current as shown in Fig. 10 and Fig. 11. Note that in the simulations described in this paper, to isolate the effect of GIDL from contributions of other body currents the impact ionization current and self-heating effect are turned off. For model without GIDL current, floating body potential (V_{body}) increases with V_{gs} at constant V_{ds} in the high bias regime due to an increase of the I_{gb} current. While for model with GIDL taken into account, the reverse bias body current initially decreases with V_{gs} due to a reduction of GIDL current at lower V_{dg} . Therefore, V_{body} also decreases with V_{gs} until the effect from the diode and I_{gb} current dominates (Fig.

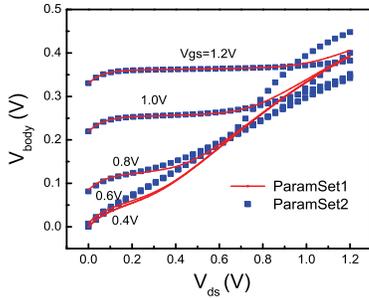


Figure 10: The floating body potential as a function of drain biases.

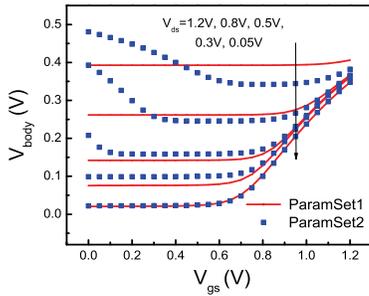


Figure 11: The floating body potential as a function of gate biases.

11).

4 CIRCUIT SIMULATION RESULTS

A 17 stage gate-loaded inverter chain is simulated using the models described above to examine the effects of the GIDL current modeling on ring simulations. Using a train of pulses with a rise time of 0.04nS as the input, the 1st switch pull-up delay, pull-up history, and AC floating body potential before the 1st and 2nd switches are measured for the PFET device. The pull-up delay is taken as from the time of the 1st falling pulse of the input of stage 10 reaches $0.5V_{DD}$ to the time the output rising pulse of stage 10 first reaches $0.5V_{DD}$. The 2nd switch delay for the PFET was measured at stage 9 when the input of stage 9 starts from low to high and then from high to low again. The pull-up history is defined as

$$H = (\tau_{1st} - \tau_{2nd}) / \tau_{1st} \cdot 100\%. \quad (3)$$

The results are given in Table 1.

The initial floating body potential of the PFET is defined by the forward and reverse leakage of the junction and is similar to the body potential obtained in Fig.11 at high drain biases. For model with GIDL current, high GIDL current flows through the junction which re-

Table 1: Ring simulation results with different models

PFET	ParamSet1	ParamSet2	Delta
Pull-up Delay (ps)	8.114	7.125	-12.2
Pull-up History (%)	2.4	-12.1	-14.5
Vbody_1st (mV)	298	421	122
Vbody_2nd (mV)	302	296	-6
Delta_Vbody (mV)	4	-124	-128

sults in a higher floating body potential during simulation compared to the model without GIDL. Similar second switch Vbody is obtained using two different models since the second switch Vbody is mainly a balance of the effect of gate-to-body tunneling current, forward diode current and capacitive coupling, which are the same between them. The second switch Vbody is lower than the first switch Vbody in the model results with GIDL included owing to a lower I_{gb} current compared to the GIDL current in the model. The reduction in Vbody of the PFET also leads to a longer delay time for the 2nd switch, therefore a negative history in the model with GIDL.

5 CONCLUSION

GIDL current can dominate the junction leakage even in the device active operating region in 45nm PDSOI technology for P-type MOSFETs. A model with GIDL included represents a higher floating body potential at low gate and high drain biases compared to that obtained using a model without GIDL. Subthreshold current and therefore off leakage can also be substantially higher than model results without GIDL. The change in the output characteristics and floating body potential with different GIDL components affects both history and ring delay time in a digital circuit. It is concluded that even for digital circuit simulations in 45nm PDSOI, GIDL current needs to be accurately modeled for leakage and speed optimizations.

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