An Accurate and Versatile ED- and LD-MOS Model for High-Voltage CMOS IC SPICE Simulation

Bogdan Tudor, Joddy W. Wang, Bo P. Hu, Weidong Liu, and Frank Lee

Synopsys, Inc., 700 E. Middlefield Road, Mountain View CA, U.S.A.
Bogdan.Tudor@synopys.com

ABSTRACT

This paper presents a high-voltage compact MOSFET model that has been proven physically accurate and numerically robust for various generations of high-voltage ED (extended drain) and LD (laterally double diffused) production CMOS process technologies. The model takes into account elegantly in formulation almost all of those physical effects identified for high voltage MOSFET operation. They include, but are not limited to:

- Quasi saturation.
- Bias-dependent, symmetric or asymmetric non-linear source and drain resistances.
- Self heating.
- Impact ionization in the drift region.
- LDMOS-specific charging effects.
- Asymmetrical charge response and transport for the forward- and reverse-mode operations of asymmetrical LDMOS.

Keywords: high-voltage MOSFET, HVMOS, LDMOS, EDMOS, compact model.

1 INTRODUCTION

The denomination "High Voltage MOSFET" encompasses a large class of devices used in many different application areas. These can vary from integrated, medium power, to discrete, very high power devices. Typical biases range from less than 10V to over 1000V. Based on the process, device types are classified as LD, ED or V (vertical) MOSFETs. The significant differences between various structures make the effort of developing a generic compact model particularly challenging. Moreover, the high voltage of operation and the presence of self-heating are susceptible to result in more circuit simulation convergence problems than in the case of low-power CMOS.

The physics and operation of such devices has been well studied (see for example [1, 2]). Several attempts to develop compact models [3, 4, 5] or macro-models [6, 7] have been made in recent years. However, while most of these attempts are oriented towards LD-MOSFETs, symmetric and asymmetric ED devices have received less attention. Also, at higher voltages, the phenomena occurring in the low doped drain (LDD) region become increasingly difficult to model accurately. Such cases often require adding extra circuit elements (macro-modeling), overcomplicating the netlist. In addition, some of the existing models account for the characteristic HV effects mostly in an empirical manner. This in turn leads to model accuracy and scalability problems.

2 MODEL DEVELOPMENT

Our proposed model is constructed to be able to reproduce the particular nature and characteristics of HV MOSFET devices by a set of mathematical and physical formulations obtained from solving the Poisson and drift-diffusion equations. In addition, the process parameters and the topological device structure are maximally incorporated in the model. For instance, the drain drift resistance, a key component in the device design and optimization for the best possible current driving capability and electrical breakdown, is connected to the intrinsic channel through an internal topological node that accurately tracks the dynamic partitions of charges, highly non-linear channel and drain resistances, and impact ionizations, all between the intrinsic and extrinsic device actions. This treatment is demonstrated to be pivotal in satisfying the strict requirements of the modeling accuracy, scalability, and numerical efficiency for production use.

The main goal we set for our model was the ability to handle both ED- and LD-MOSFET devices in all modes of operation, including reverse-mode and self-heating, with comparable accuracy, and in an entirely compact formulation. Thus, the starting point in developing the model was to combine the features of the two main device types and to come up with a unified, conceptual device structure. This was further decomposed in basic physical elements from which the model topology was derived. Figure 1 illustrates a simplified topology that includes an internal MOSFET model and independent models for the drain and source resistances of the device, respectively.

2.1 Model basis

We selected the BSIM4 model [8] as a foundation for the internal MOSFET in the topology. We have decided to do so because BSIM4 is a robust and mature model, having

been the standard in the semiconductor industry for many years. This helped us to comprehensively cover the behavior of the internal MOSFET device, including temperature and geometry scaling. Advanced RF-related effects, such as non-quasi-static (NQS) and RF-related bias-dependent RG models are also built in.

2.2 HV-MOS specific model features

A number of extra elements and model equations have been added, to accurately account for the particular physics of the device:

- Self-heating network, with scalable and temperature-dependent elements.
- Asymmetric diode models, including carrier recombination and tunneling components.
- Substrate current, including impact ionization at the drain of the internal MOSFET and impact ionization in the drift region (see Fig. 5a-b).
- Accurate temperature equations.
- Handling of reverse-mode of operation, for asymmetric devices.
- LDMOS-specific charge and capacitance model.

2.3 TCAD simulations

Extensive TCAD simulations were designed, in order to provide one with deeper insights into the microscopical physical processes of electric potential and charge distributions in the high field regions inside the device. By taking advantage of the unique insight of TCAD device simulation, several key quantities of the HV MOSFET were separately tested and validated, and the corresponding model equations have been refined:

- The drain and source resistances and their dependence on bias and temperature (Fig. 2a-b).
- Confirmation of the internal drain and source voltage values (Fig. 3a-c).
- The characteristic capacitance behavior of LDMOS devices (Fig. 4).

3 PARAMETER EXTRACTION

A global parameter extraction approach, customized to our model's features, has been developed. The procedure, based on optimization, simultaneously uses data measured on multiple device geometries, at different temperatures. The flow starts with the extraction of current equation parameters in the linear region, followed by the saturation region. At this point, reverse-mode data can be also used, if available, for a better characterization of asymmetric devices. Substrate current measurements are included here as well. To allow the accurate extraction of self-heating-related parameters, some of the temperature coefficients are optimized together with the room temperature parameters by using data available at all temperatures.

For the best possible accuracy in the extraction of the specific LDMOS capacitance parameters, optimization based on both C-V and I-V data is recommended, some of the key I-V model parameters being refined this way.

In order to preserve the physical character of model equations this global extraction approach is recommended, but binning is also available, as an alternative.

4 MODEL VALIDATION

The model has been validated based on a wide range of devices and technologies, with gate oxide thicknesses ranging from below 10nm to over 100nm and with the drain bias from a few volts up to several hundreds of volts. Symmetrical and asymmetrical ED-MOS and LD-MOS devices have been characterized and extracted with excellent accuracy without having to use binned models. The model proved to be accurate for high voltage devices, with no need for external circuit elements.

Figure 6a-c illustrates the accuracy of the model in handling the typical behavior of HV MOSFETs, including impact ionization, quasi-saturation and self-heating.

5 CONCLUSION

We have developed a compact model that is applicable to both LD- and ED-MOSFET devices. This model has consistently demonstrated very good accuracy and scalability over bias, geometry and temperature, without the need for binning or macro-modeling. The model has already been successfully used in industrial production.

REFERENCES

[1] Y. Kim et al, "New physical insights and models for high-voltage LDMOST IC CAD," IEEE Trans. ED, vol. 38, no. 7, pp. 1641–1649, Jul. 1991.

[2] C.M. Liu, J.B. Kuo, "Quasisaturation Capacitance Behavior of a DMOS Device", IEEE Trans. ED, vol. 44, no. 7, pp. 1117-1123, July 2007.

[3] A. Aarts et al, "A Surface-Potential-Based High-Voltage Compact LDMOS Transistor Model", IEEE Trans. ED, vol.52 no.5, pp. 999-1007, May 2005.

[4] Z. Liu, "High-Voltage Applications Demand a Robust HVMOS Device Model", Avant! Electronics Journal, December 1998, pp. 16-19.

[5] N Hefyene et al, "EKV compact model extension for HV lateral DMOS transistors", Proceedings of ASDAM 2002, pp. 345 – 348.

[6] J. Jang et al, "Circuit model for power LDMOS, including Quasi-Saturation", Proceedings of SISPAD 1999, pp. 15-18.

[7] E.C. Griffith et al, "Capacitance Modelling of LDMOS Transistors", Proceedings of ESSDERC 2000, pp. 624 – 627.

[8] "BSIM4.6.0 MOSFET Model User's Manual", University of California Berkeley, 2006.

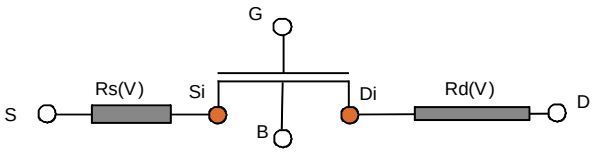


Figure 1. Simplified model topology.

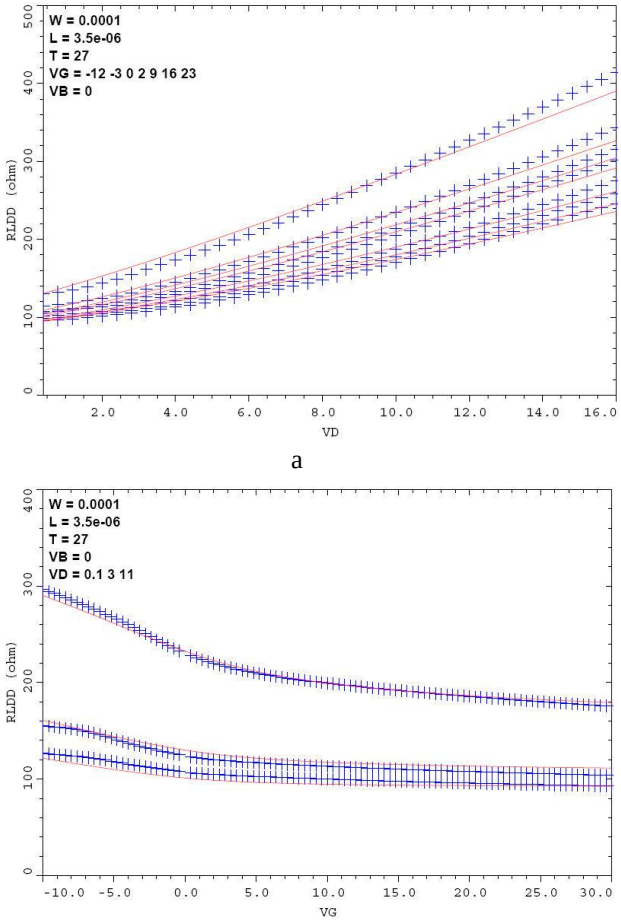


Figure 2. R_{LDD} model versus Medici LDD structure simulation: V_D dependence (a) and V_G dependence (b). Symbols: Medici. Lines: model.

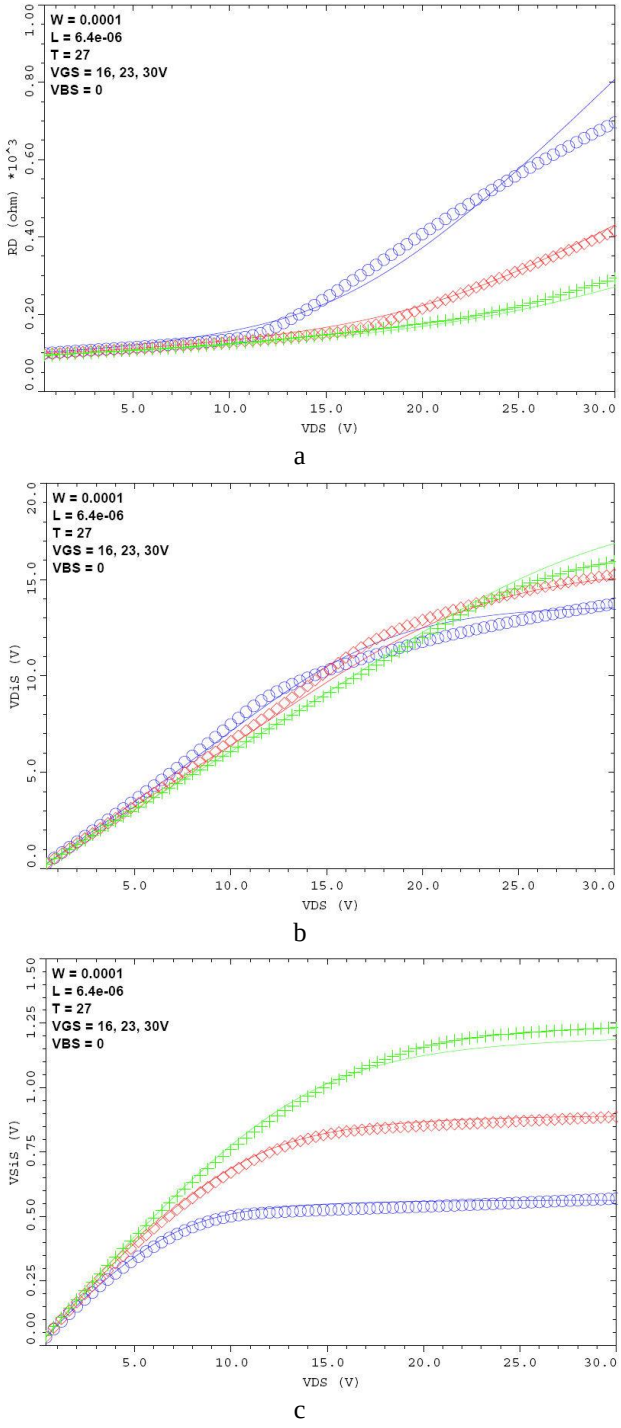


Figure 3. Model verification against Medici HVMOS structure simulation: $R_D(V_{DS})$ (a), $V_{DiD}(V_{DS})$ (b), and $V_{SiS}(V_{DS})$ (c). Lines: model. Symbols: Medici (+: V_{GS}=16V, ◊: V_{GS}=23V, O: V_{GS}=30V).

NSTI-Nanotech 2008, www.nsti.org, ISBN 978-1-4200-8505-1 Vol. 3

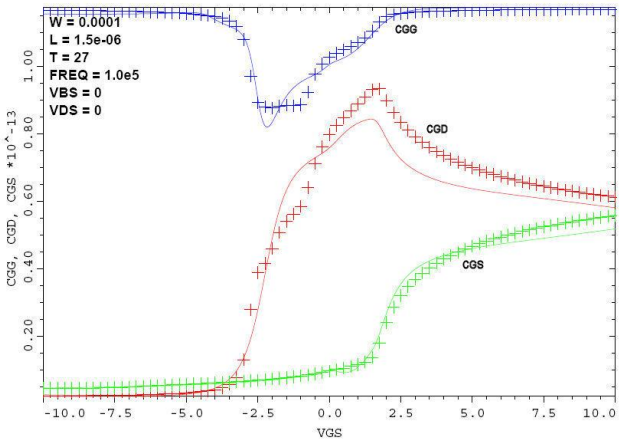
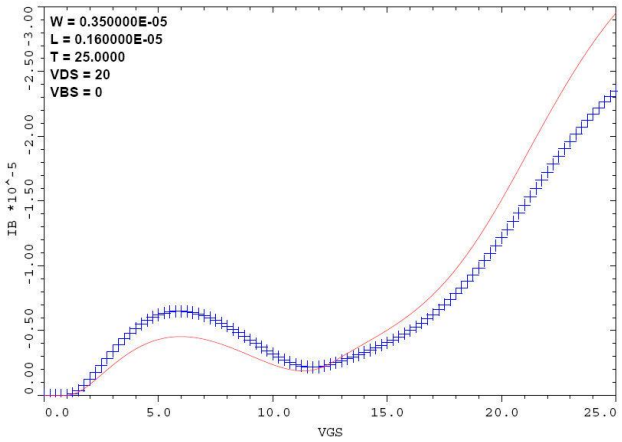
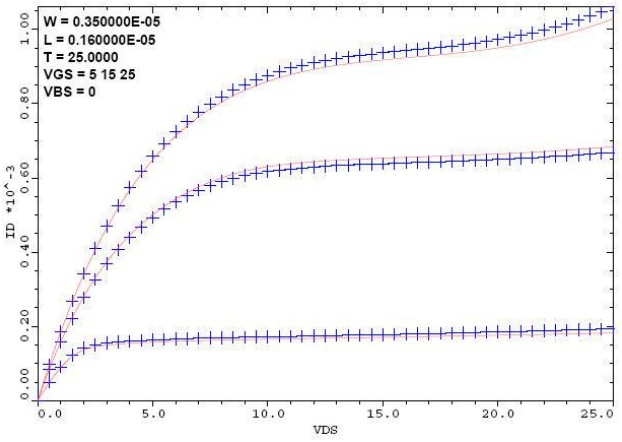


Figure 4. LDMOS C(V) model against Medici simulation. Symbols: Medici. Lines: model.

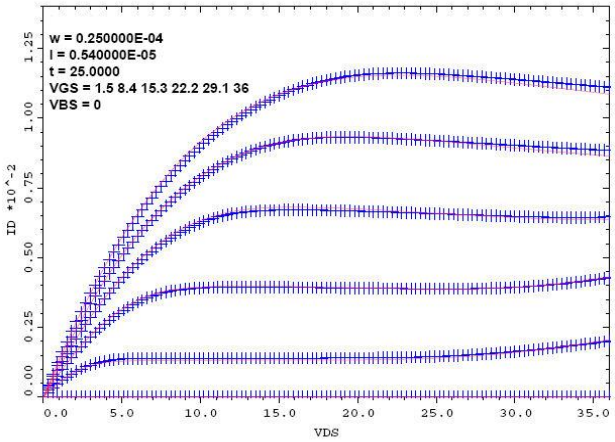


a

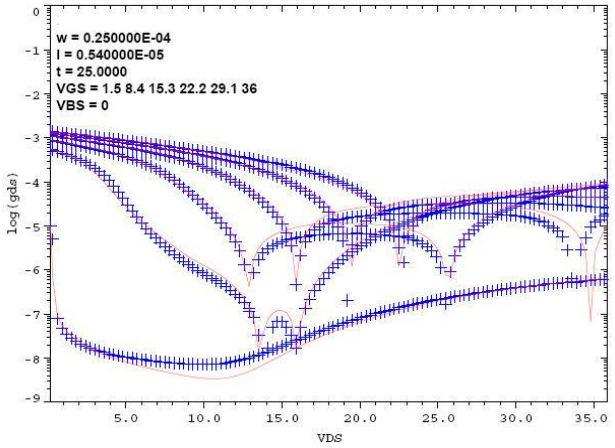


b

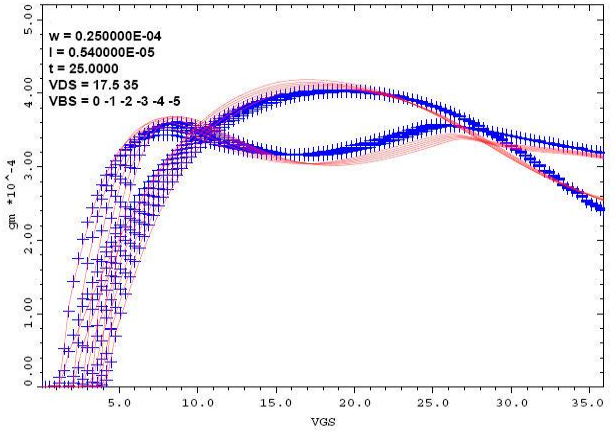
Figure 5. Impact ionization in the drift region: effect on I_{SUB} (a) and on I_D (b).
Symbols: measured data. Lines: model.



a



b



c

Figure 6. Simulated versus measured data: $I_D(V_{DS})$ (a), $g_{ds}(V_{DS})$ (b), and $g_m(V_{GS})$ (c).
Symbols: measured data. Lines: model.