Hybrid Semiconductor/Nanoelectronic Circuits

Konstantin K. Likharev
Stony Brook University, Stony Brook, NY 11794-3800, U.S.A., klikharev@notes.cc.sunysb.edu

ABSTRACT

This is a very brief review of the recent work on the development of hybrid semiconductor/nanodevice integrated circuits. Such a circuit will combine a CMOS subsystem, and a nanowire crossbar with simple bistable two-terminal devices formed at each crosspoint, connected with an area-distributed "CMOL" interface. Simulations have shown that the hybrid circuits may serve as the basis for (i) terabit-scale memories with access time below 100 ns and defect tolerance up to 10%, (ii) FPGA-like reconfigurable logic circuits with density at least two orders of magnitude higher than that of CMOS FPGAs, and (iii) mixed-signal neuromorphic networks ("CrossNets") which may become the first hardware basis for challenging the human cerebral cortex in both areal density and speed. Recently the work on the hybrid CMOS/nano circuits received a strong boost from the experimental demonstration of reproducible metal-oxide devices and nanowire crossbars with 15-nm-scale half-pitch.

Keywords: nanoelectronics, CMOL, memory, logic, mixed-signal neuromorphic networks

1 INTRODUCTION

The exponential ("Moore's-Law") progress of semiconductor digital integrated circuits [1] has enabled all the current information technology revolution. However, it is generally accepted now that this progress will turn into a crawl some time during the next decade. The most fundamental reason of this anticipated crisis is that the workhorse device of these circuits, the silicon field-effect transistor, requires an accurate lithographic definition of several dimensions including the length and width of its conducting channel. As these devices are scaled down, arising quantum mechanical effects require the definition to be much more precise [2], which in turn requires much more expensive lithography tools. At some point the scaling will start bringing diminishing returns. Unfortunately, candid estimates show [1, 2] that alternative electronic devices either run into similar fabrication problems, or have lower functionality, or both.

2 CMOS/NANO HYBRIDS: DEVICES

However, recent experimental and theoretical research results (notably those published during the past 18 months) indicate at least one plausible means to avoid the impending crisis: hybrid semiconductor/nanodevice circuits [2-4] in which a silicon chip is augmented with a top layer of simple (two-terminal) but very small nanodevices. The main idea of this paradigm is that the two-terminal devices have only one critical dimension (distance between two electrodes) which can be readily controlled, with sub-nanometer precision and without overly expensive equipment, by film thickness.

Simple two-terminal devices cannot amplify signals as transistors; however, they may have the "latching switch" (a.k.a. "programmable diode") functionality – see Fig. 1a. At low applied voltage, such device operates as a diode, i.e. has a nonlinear monotonic *I*-*V* curve, but high voltages switch it from this "ON" state into the virtually nonconductive "OFF" state and back. This means, in particular, that the device can operate as a memory cell storing one bit of information in its internal state.

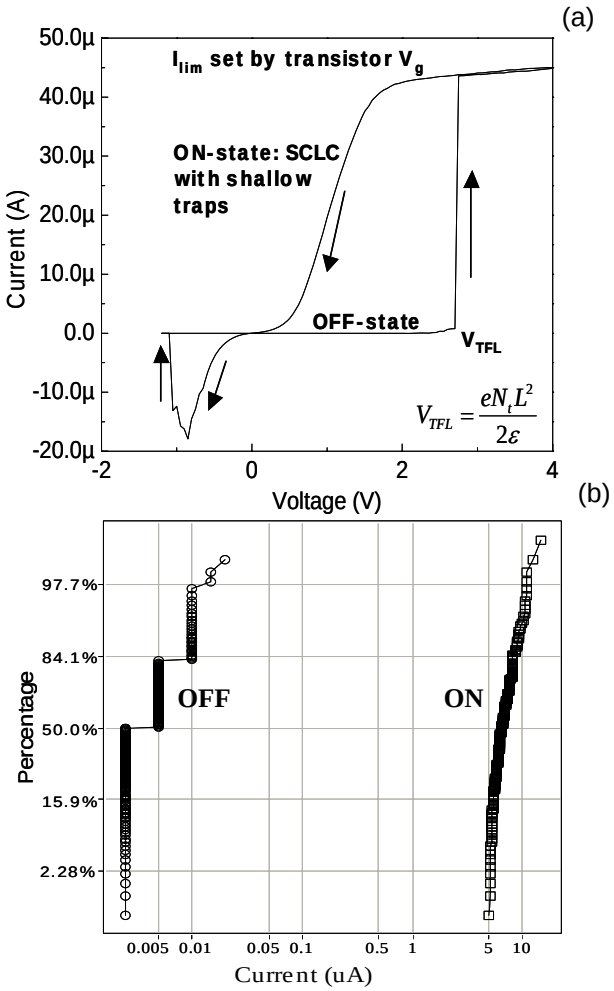

Figure 1: Latching switch based on a few-nm-thick CuO_x layer: (a) a typical *I*-*V* curve and (b) the statistics of the OFF and ON current distribution [5].

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Devices of this type have been demonstrated using several other structures: organic films (both with and without embedded metallic clusters), self-assembled molecular monolayers, and thin chalcogenide and crystalline perovskite layers. The physics of bistability of most devices it not quite clear, and there are reasons to believe that they may not be scalable below ~10 nm. (The excellent reproducibility shown in Fig. 1b is for relatively large, 180×180 nm^2 junctions.)

This problem may be addressed in future using uniform self-assembled monolayers of specially designed molecules [6] implementing single-electron latching switches [7].[1] A major challenge on this way is the reproducibility of the interface between the monolayer and the second (top) metallic electrode, because of the trend of the metallic atoms to diffuse inside the monolayer during the electrode deposition. Recent encouraging results towards the solution of this problem have been obtained using an intermediate layer of a conducting polymer [9].

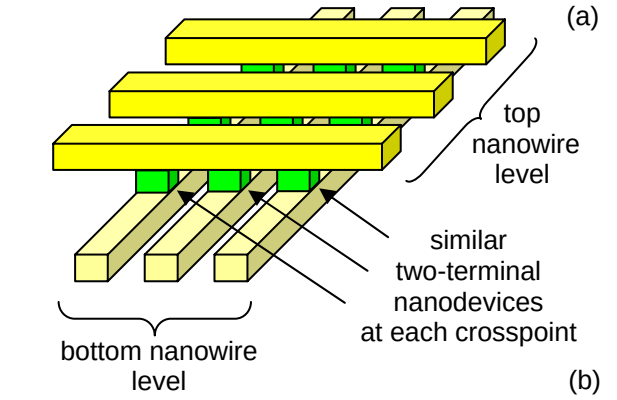
3 NANOWIRE CROSSBARS

For efficient operation, the nanodevices, with their miniscule footprint, have to connected by nanowires to each other and to the silicon transistor subsystem. Figure 2 shows the topology which is the focus of most current research work in this field [2-4]: similar latching switches are formed at each crosspoint of a nanowire crossbar. The advantage of this configuration is that it does not require alignment between the two nanowire levels, and hence may be fabricated by prospective patterning techniques such as nanoimprint. This technique has already allowed demonstrations of crossbars with 15-nm-scale half-pitch [10, 11] (Fig. 2b), and may be scalable all the way down to a few nanometers.

4 CMOL INTERFACE

Still, the crossbar geometry pushes the silicon/nanodevice interface challenge only one step further, because an individual access to each crosspoint nanodevice still requires an individual assess to each nanowire. Several sophisticated techniques based on stochastic doping of semiconductor nanowires have been suggested for this purpose [3]; however, the recently suggested "CMOL" interface [2, 4] seems more general and easier for implementation. In this approach (Fig. 3) the silicon/nanowire interface is provided by sharp-tip pins which are distributed all over the circuit area. (Such pins have already been demonstrated experimentally in the context of field-emission arrays.)

The main trick here is the rotation of the nanowire crossbar by a certain angle relative to the rectangular grid of pins (Fig. 3b), which allows the CMOS subsystem to contact each and every nanowire and hence address each individual nanodevice. Even more remarkably, nanoscale alignment of the crossbar with the CMOS stack is not required for high circuit fabrication yield.



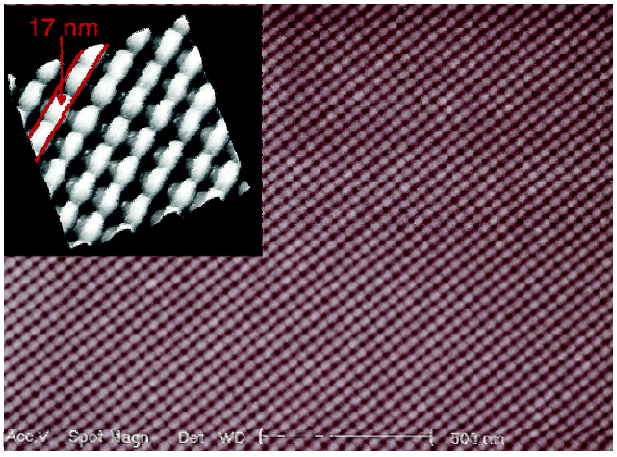


Figure 2: Nanowire crossbar: (a) general scheme and (b) an experimental sample with F = 17 nm [10].

The simplified version of the CMOL interface, suggested recently [12], would reduce the circuit density rather significantly, but still may be beneficial for first practical demonstrations of the CMOS/nano hybrids.

5 APPLICATIONS: MEMORIES

Recent detailed calculations have shown that the hybrid CMOS/ circuits with crosspoint latching switches may be used to move well beyond the usual ("CMOS") silicon electronics in virtually all areas of information processing and storage. First of all, they may enable terabit-scale resistive memories with sub-100-ns assess time [13]. Figure 4 shows the calculated normalized density of such memories as a function of bad (stuck-on-open) crosspoint

[1] Metal-based, low-temperature prototypes of such switches, with multi-hour retention times, have been demonstrated experimentally [8]. However, so far molecular implementations have been only demonstrated for the main components of these devices, single-electron transistors.

devices. One can see that, in addition to ultrahigh density, the memories may be rather defect-tolerant, provided that an optimized synergy of bad bit exclusion and advanced error-correction codes [13] has been used.

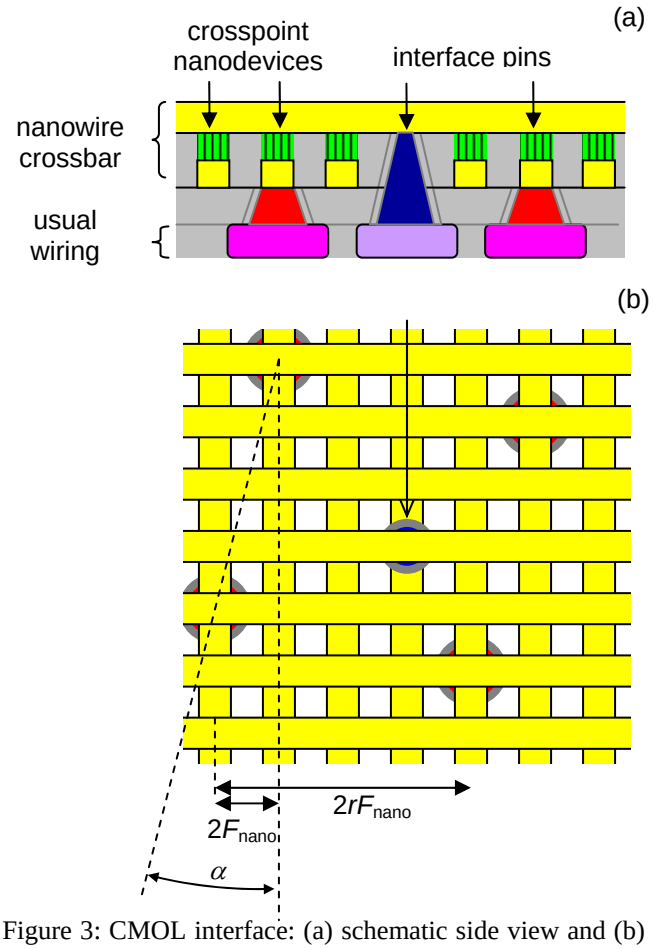


Figure 3: CMOL interface: (a) schematic side view and (b) top view. The specific rotation angle $\alpha = \arctan(1/r)$, where r is an integer, makes each nanowire individually accessible from the semiconductor-transistor subsystem.

6 APPLICATIONS: DIGITAL LOGIC

Even more importantly, reconfigurable hybrid logic circuits may provide function density at least two orders of magnitude higher than that of their CMOS counterparts fabricated with same design rules, at manageable power dissipation and comparable logic delay. It is remarkable that this performance may be combined with a defect tolerance even higher than that of the resistive memories [14-16]. Figure 5 shows the area-by-delay product of two representative hybrid logic circuits as a function of the nanowire half-pitch, for several values of the CMOS half-pitch.

Preliminary estimates show that even higher performance may be obtained using crosspoint devices with negative-differential-resistance (NDR) branches, which allow signal restoration in the nanodevice subsystem.

7 MIXED-SIGNAL NETWORKS

Finally, in the long run, the most important application of the hybrid CMOS/nanodevice circuits may be mixed-signal neuromorphic networks – "CrossNets" [6, 7, 16-18]. Simulations have shown that such circuits, trained as pattern classifiers, may used, for example, for reliable recognition of a human face in a large crowd at a speed making online operation feasible [17]. (At the same time, CrossNets are even more defect-tolerant than the digital hybrid circuits.)

In the long run, the CrossNets may become the first hardware capable of challenging human cerebral cortex in density, far exceeding it in speed, at comparable component functionality and acceptable power consumption [6, 16]. For this, the networks should be trained to perform advanced information processing tasks with delayed reward. The first successes on that way have already been reached [18].

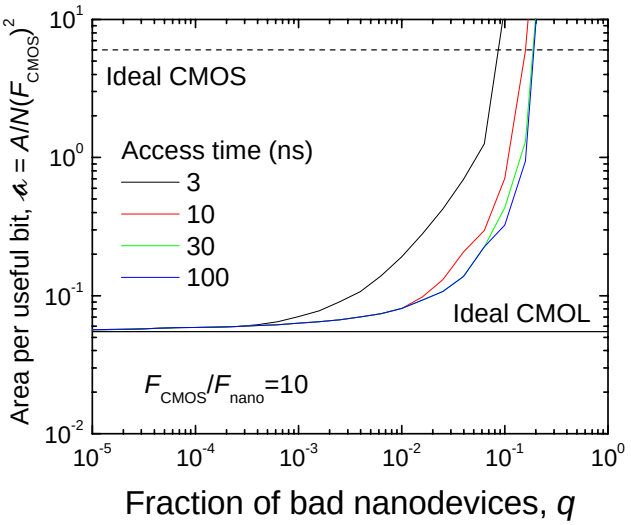


Figure 4: Calculated normalized area of resistive CMOL memories as a fraction of defective crosspoint devices, for several values of access time and the half-pitch ratio anticipated at the [13].

8 CONCLUSIONS

Just a couple years ago, it seemed [4] that the exciting prospects of hybrid CMOS/nanodevice circuit implementation depended crucially on the development of radically new, molecular technology of reproducible crosspoint devices, which could take a decade if not more. However, as a result of the recent success in fabrication of reproducible metal-oxide devices [5] and nanowire crossbars with 15-nm-scale half-pitch [10, 11], the first demonstration of hybrid integrated circuits may be just a few years (months?) away.

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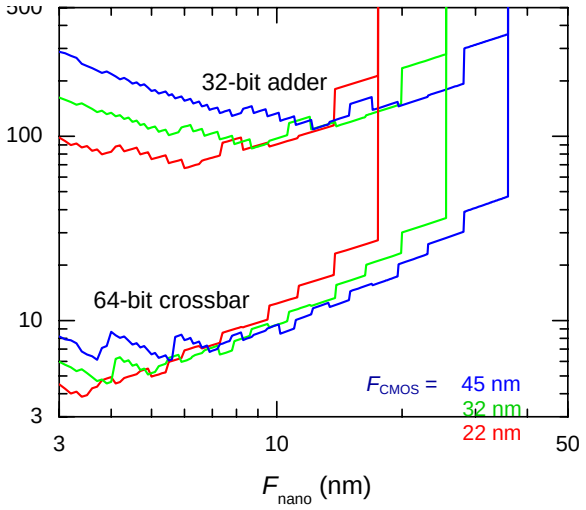

Figure 5: The calculated area-by-delay product of two digital circuits implemented using the CMOS/nano hybrids with the CMOL interface, optimized at a fixed (ITRS-specified [1]) power per unit area [14].

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