Fabrication and Modeling of CNT Field-Emission Devices

J. Koohsorkhi[*], N. Rouhi[*], Y. Abdi[*], S. Mohajerzadeh[*], M.D. Robertson[**] and R.D. Thompson[**]

[*] Thin Film and Nano-Electronics Laboratory, Nano-Electronics Center of Excellence, University of Tehran, Tehran, Iran, smohajer@tfl.ir

[**] Department of Physics, Acadia University, Nova Scotia, Canada, michael.robertson@acadiau.ca

ABSTRACT

We report the fabrication of field-emission devices based on vertically aligned CNTs that possess a novel self-defined gate structure. These devices can find application in flat-panel displays, nanolithography systems and new sensor technologies. Growth of the CNTs on Si was achieved using PECVD with nickel as the seed layer. A mixture of C_2H_2 and H_2 was used as the feed gas, the substrate temperature was 650 ^oC and the plasma power density was 4.5 W/cm^2. The Ni seed layer was patterned prior to growth of the CNTs in order to create various micro- and nano-scale geometries. The effects of the gate and anode potentials on the current-voltage behavior are discussed and a theoretical model using an expanded Fowler-Nordheim tunneling effect is presented.

Keywords: carbon nanotubes, field emission, modeling

1 INTRODUCTION

Since their discovery in 1991, carbon nanotubes (CNT's) have attracted significant attention because of their exceptional electronic and mechanical properties [1, 2]. Possessing one-dimensional structure and extraordinary electronic properties, CNTs are promising candidates for quantum wire applications [3]. CNTs behave like one dimensional quantum wires and can display either metallic or semiconducting properties depending on their chirality and diameter. Single-wall (SW) and multi-wall (MW) CNTs can be used in a wide variety of applications where mechanical durability and high current densities are required. Furthermore, SWCNTs are good candidates for energy storage and sensors because of their greater flexibility compared to MWCNTs. Other applications of SWCNTs are as channels in MOSFETs and in devices as interconnects in VLSI technology. Similarly, multi-wall carbon nanotubes are of interest in future electronic applications, such as field-emission devices, owing to their exceptional electronic properties and mechanical stability. In addition, MWCNTs and bundles of SWCNTs would be good candidates to replace copper interconnect technology in submicron VLSI because they can transport high electric currents without encountering the doping problem [4 - 6].

In addition, the field emission properties of CNTs have been studied by several researchers due to their potential application in CNT-logic devices. Field emission is the extraction of electrons from the tip of a CNT by tunneling through the surface potential barrier as the result of the application of a strong electric field. One challenging task is the large scale integration of CNTs in electronic devices [7, 8].

In this paper a novel self-defined structure for the realization of field-emission devices is reported with application to flat-panel displays, nanolithography systems and new sensor technologies [9]. The physical characteristics of the samples have been investigated using SEM, and the experimental and theoretical electrical behavior of the devices will be presented. As compared to conventional self-aligned field-emission devices where nano-lithography is usually employed to form the gate, the fabrication of the devices proposed in this paper does not require any nano-lithography step and the formation of the gate is possible through a self-defined process.

2 FABRICATION OF FIELD EMISSION DEVICES

Fig. 1a shows the processing steps for the creation of field-emission devices with a self-defined gate structure. The fabrication requires the vertical growth of CNTs by PECVD and the CVD-deposition of TiO_2 (insulator) and Cr (metal gate) layers. The metal layer is isolated from the substrate by the insulating titanium-oxide film and its position around the nanotube allows for control of the emission of electrons from the sharp tips of the nanotubes. The distance between the gate and cathode is determined by the thickness of the insulating layer and can be accurately controlled. After deposition of the oxide-metal bilayer, polishing and oxygen-plasma steps are performed in order to expose the CNT and clean the exposed surfaces. Fig. 1b shows the operation of a self-defined field-emission device where an electron beam is emitted from the self defined gated structure. The presence of the metal-insulator bilayer surrounding each individual nanotube controls the emission of electrons from its sharp tip. Since the CNT is electrically connected to the cathode via growth on the Si substrate, applying a voltage between the anode and cathode causes the emission of electrons from the CNT and a current is measured. The devices made in this manner are composed of clusters of carbon nanotubes making them suitable for use in

large area field emission applications without the use of a nanolithography step.

The growth of vertically aligned nanotubes is critical to the realization of these devices and is achieved using PECVD with nickel (t = 30 nm) as the seed layer. Hydrogenation of the electron-beam-deposited amorphous Ni layer at a temperature of 650 ^{o}C is used to form nano-sized islands of the nickel catalyst. The growth occurs in a mixture of C_2H_2 and H_2 at a pressure of 2.5 torr, a temperature of 650 ^{o}C and a plasma power density of 4.5 W/cm^2. Figure 2 shows the growth of CNTs where the Ni layer had been patterned using standard photolithography in order to obtain desired shapes and geometries of CNTs. The average length of the CNTs was about 5 microns.

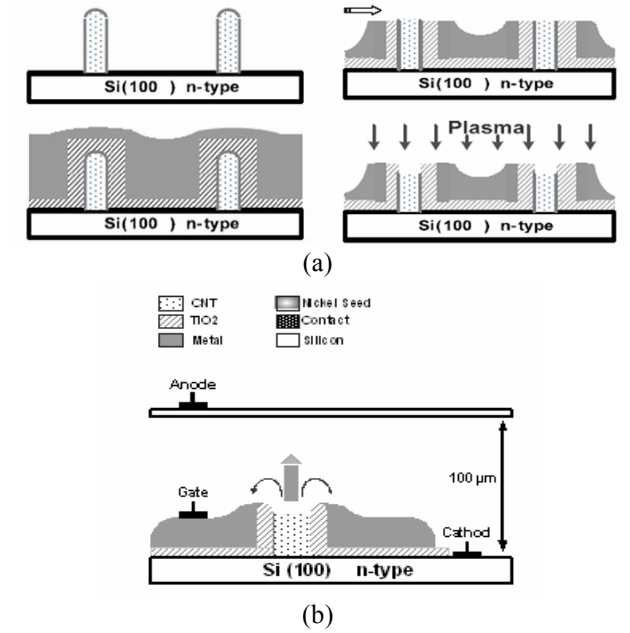

Figure 1: (a) The processing steps applied to CNTs in order to form self-defined gated field-emission devices. (b) Operation of a field-emission device displaying the anode, cathode and gate connections.

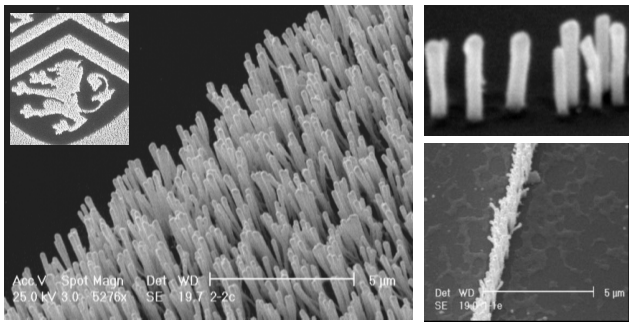

Figure 2: SEM images of patterned vertically aligned CNTs grown on a Si substrate.

Fig. 3 presents SEM images of the structure after 200 nm of TiO_2 has been deposited on the CNTs. The thickness of the TiO_2 layer is an important factor in controlling the current-voltage characteristics of the fabricated devices which have been examined theoretically in the model proposed in Section 4. Subsequently, a metal layer is deposited for use as a gate and then the structure is polished and plasma ashed in order to expose the embedded carbon nanotubes and to make the operation of the device feasible. Fig. 4 presents SEM images of individual CNTs before processing (left) and after completion of the fabrication process (right).

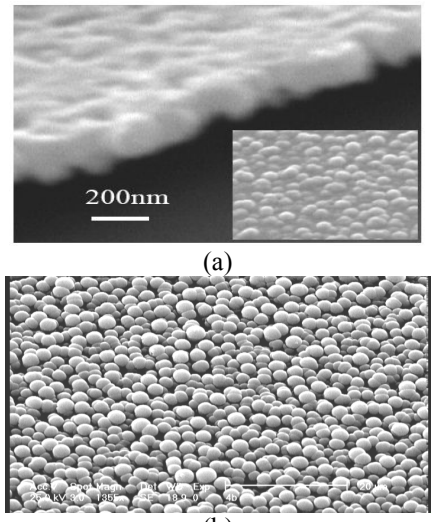

Figure 3: (a) cross-sectional and (b) planview SEM images of CNTs after deposition of the TiO_2 layer by CVD.

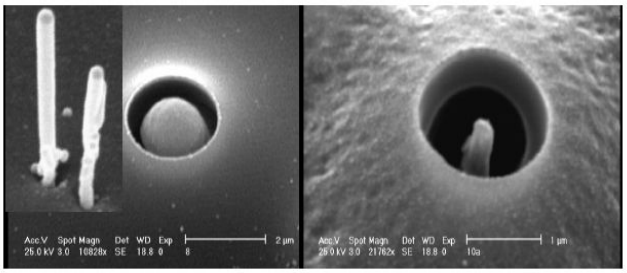

Figure 4: SEM images of the initial (left) and encapsulated (center and right) CNTs after polishing and plasma ashing.

3 EXPERIMENTAL RESULTS AND DISCUSSION

The electrical characterization of the tubes was performed using a Keithley-K82 parameter analyzer. Fig. 5a shows the current-voltage characteristics of the device measured at four distances between anode and the cathode, and Fig. 5b shows the current versus gate voltage relationship highlighting the fine control of the gate over the emission current. From Fig. 5, it is observed that the anode-cathode (A-C) voltage has little effect on the current at intermediate voltages and the gate is the primary controller of the current. This behaviour is similar to the saturation region of field-effect transistors. At A-C values below about 12 volts, a significant drop in the measured current of the transistors is observed. At lower A-C voltages, the

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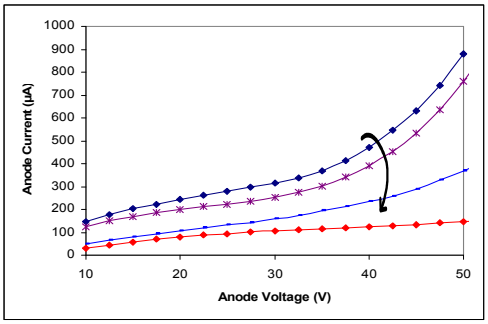
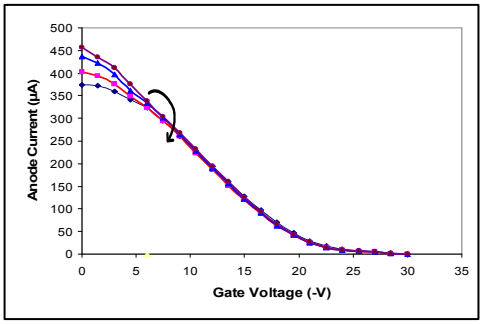
current depends on the A-C voltage, displaying a more linear regime of operation.



(a)



(b)

Figure 5: Electrical characteristics of the fabricated devices for anode-cathode distances of 120, 130, 140, and 150 µm where the arrow points towards increasing A-C distance. (a) Current vs. anode voltage curves, and (b) the effect of the surrounding gate potential in controlling the current.

Fig. 6 shows the I-V characteristic of a device where the distance between anode and cathode was 100 µm and saturation in the anode current is observed. The I-V characteristics of these devices can be explained considering the series of schematic diagrams presented in Fig. 7. For a given A-C voltage, the negative potential applied to the gate leads to a focusing of the electrons emitted from the tip of the CNTs. If the distance between the anode and cathode is less than the distance to the focusing point, the effect of the A-C voltage on the current is significant and a linear relation is observed. However, if the anode is above the focusing point, the current is almost constant and the A-C voltage shows less effect on the emission current. This effect is similar to channel formation in JFETs. By increasing the gate voltage further (negative polarity), the focusing occurs closer to the cathode electrode and eventually no electron extraction is possible, turning off the device.

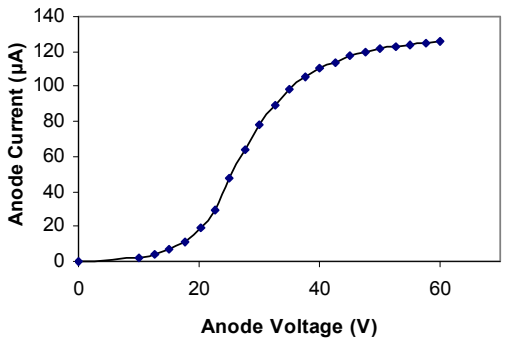


Figure 6: I-V behavior of a device where the distance between the anode and cathode was set at 100 µm. Three regions: sub-threshold, nearly linear and saturation are observed.

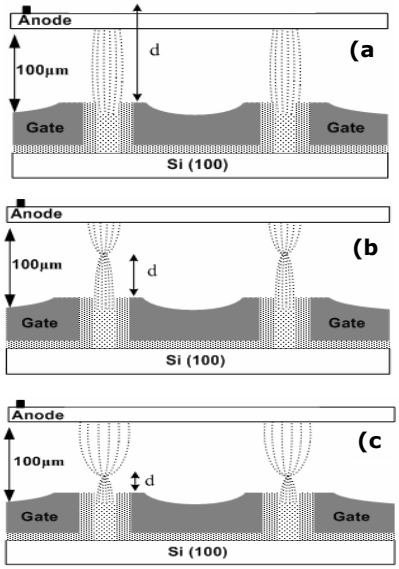
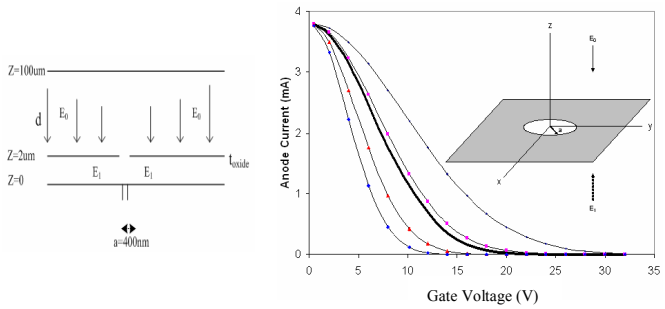


Figure 7: Schematic diagram of the proposed mechanism of device operation. At small anode-cathode spacing, the focusing point for the emitted electrons is above the anode plate and the A-C voltage has a significant effect on the current. At a higher gate voltage, this focusing occurs at smaller distances and emission current is reduced. At still higher gate voltage, electron extraction is limited and an OFF state results.

4 DEVICE MODELING

In this section, a theoretical model for the electrical behavior of the device is proposed. Emission of electrons from the tip of the CNT is due to tunneling and Fowler-Nordheim behaviour has been observed in changes in emission current as a function of potential in agreement with other results presented in the literature [10].

In order to model the I-V characteristic of our devices, we have solved for the electric field distribution using Poisson's equation for the approximate structure shown in Fig. 8a. Both Dirichlet and Neumann boundary conditions were applied for obtaining the electric field components around the CNT tip.



(a) (b)

Figure 8: (a) Geometry of the device structure used in the modeling. (b) Theoretical modeling results showing the effects of the gate voltage on emission current. Oxide layer thicknesses of t = 100 nm, 150 nm, 200 nm and 250 nm are represented by blue diamonds, red triangles, purple squares and dark blue dots, respectively.

With no gate voltage applied, one can obtain the anode current as a function of V_{AC} from the Fowler-Nordheim equation [10],

$$I = 2.34\times10^{-4}\times(\Phi/e)^{3/2}\times V_{AC}^{2}\times\exp\left(\frac{-6.88\times(\Phi/e)^{3/2}}{V_{AC}}\right)(A) \qquad (1)$$

where Φ is the work function of the CNT with a value between 4.6 - 4.9 eV. After incorporating the effects of the gate potential, V_g, on the total electric field one can obtain the following expression for the emitted current,

$$I = 1.4\times10^{-3}\times\exp\left\{1-[(1-\frac{V_g}{\eta E_o t})(2.65\times10^{2})]^{2}\right\}(A) \qquad (2)$$

where η is a normalization factor of the electric field near the gate-plane which equals 5.7×10^{-4} and the numerical factor in the exponential term was obtained analytically. Using $E_0 = 5\times10^{5}$ V/m, the anode current becomes

$$I = 1.4\times10^{-3}\times\exp\left\{1-[(1-\frac{2.85\times10^{2}V_g}{t})(2.65\times10^{2})]^{2}\right\}(A) \qquad (3)$$

Eqn-3 gives the anode current as a function of V_g and the thickness of the TiO_2 layer, t. Fig. 8b shows the theoretical results for four thicknesses of the gate oxide layer and the corresponding experimental data (thick, solid line). A reasonable fit is observed between the experimental data and the curve calculated from eqn. 3 provided a thickness of 200 nm is assumed for the insulating layer. This value for the oxide thickness is consistent with that observed in Fig. 3a. From this model, one can observe that a lower oxide thickness yields a higher slope of the gate control on the emission (anode) current.

5 SUMMARY AND CONCLUSION

In summary, we have successfully fabricated and tested field emission devices and transistors using a novel self-defined structure based on encapsulated vertically aligned carbon nanotubes. The electrical characteristics of these structures have been investigated and excellent control over the emission current by the gate has been observed. A theoretical model has been developed which incorporates the tunneling effects expressed in the Fowler-Nordheim equation and the effects of the gate using electromagnetic theory to obtain a closed form equation for the emission current as a function of gate and anode-cathode voltages.

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