A Study on the Electrical Properties of Plasma Nitrided Oxide Gate Dielectric in Flash Memory

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ABSTRACT

In this paper, we address the effect of Plasma Nitridation on the gate dielectric in terms of device characteristics of NMOS/PMOS transistor. Firstly, boron segregation due to Plasma Nitridation near Si/SiO_2 interface and bulk Si is experimentally characterized by 1D SIMS, and its profile is reproduced in simulation of which parameters for boron diffusion are accurately calibrated through comprehensive calibration process. Secondly, the electrical behavior of NMOS/PMOS transistor with plasma nitride gate dielectric is verified, observing uncommon behavior of C-V diagram in the case of buried-channel PMOS transistor. And, we prove that excessive amount of interface traps generated by Plasma Nitridation influences abnormal electrical behavior of NMOS/PMOS transistor.

Keywords: dry oxidation, plasma nitridation, process simulation, boron segregation, C-V diagram.

1 INTRODUCTION

Plasma Nitridation provides strong immunity to boron penetration of p+ poly gate and incorporates nitrogen (N) atoms at Si/SiO_2 interface which improve hot carrier resistance, leakage current and stress immunity. This principal advantage of plasma nitrided gate dielectric over conventional oxynitridation with NO or N_2O has motivated much work on its utilization, and plasma nitridation is now regarded as a promising technology for a reliable gate insulator for electrical erasable nonvolatile memory such as Flash Memory [1,2]. However, there remain many issues to be addressed if its electrical characteristics are concerned [3]. One of the issues is the dopant segregation of additional annealing process of Plasma nitridation, which changes the electrical property of cells and peripheral transistors. Another problem is the effect of the positive charge trap mainly generated in Si/SiO_2 interface where ion damage of Plasma Nitridation is maximized. In this paper, we address the effect of Plasma Nitridation on the gate dielectric by a combined experimental and simulation study of gate oxidation.

2 EXPERIMENTS AND SIMULATIONS

Samples needed for this study are fabricated with the same process for the fabrication of 63nm NAND flash cell transistor [4]. BF_2 dose ($7\times10^{12}cm^{-2}$) for NMOS transistor and BF_2 dose ($1\times10^{13}cm^{-2}$) for PMOS transistor are implanted separately at low energy (20KeV) through a screen oxide. After screen oxide removal, gate oxidation is performed to grow 80A oxide with temperature of 900°C for about 60 minutes. Poly-Silicon is used as gate material and aluminum is used for metal electrode.

2.1 Boron Segregation

Firstly, Boron segregation at the Si/SiO_2 interface and boron diffusion in silicon is experimentally characterized by means of 1D SIMS. Samples with various gate oxidations are prepared with the same process conditions as listed in Table.1. After growing gate dielectric by dry oxidation, NO Anneal and Plasma Nitridation are applied on samples selectively.

Sample	Oxidation	Plasma Nitridation
SA1	Dry Oxidation	X
SA2	Dry Oxidation	O
SA3	Dry Oxidation + NO Anneal	X
SA4	Dry Oxidation + NO Anneal	O

Table.1 Samples used to study segregation during gate oxidation

As shown in Fig.1 depicting boron concentration profile acquired by high-resolution 1D SIMS, boron concentration between dry oxidation only samples and NO anneal additional samples possess different profile. Thus, it is confirmed that plasma nitrided gate dielectric possesses the same boron concentration profile on Si as the gate dielectric with dry oxidation, meaning no additional boron segregation of Plasma Nitridation.

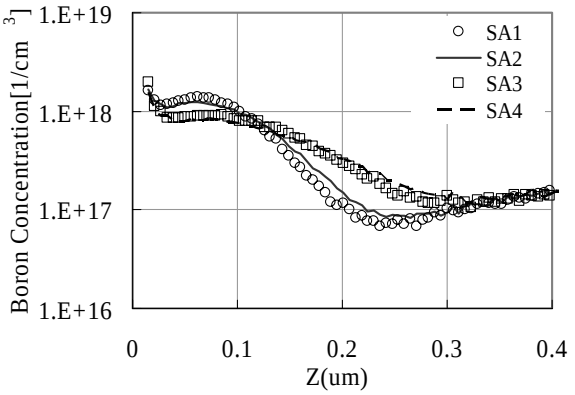

Fig.1 SIMS profiles for samples with gate oxidation

2.2 3-D Simulation Calibration

Secondly, a comprehensive process simulation model is accurately calibrated and then exploited to investigate the dependence of device electrical parameters on NMOS/PMOS Transistors. As shown in Fig.2, 2-D and 3-D process simulation are performed with ENEXSS tools and device simulation is performed with Synopsys tools [5]. For accurate simulation, critical physical dimensions such as Lengh/Width of transistor and tunnel oxide thickness are measured by SEM and TEM. To extract process simulation model parameters (boron segregation, OED(Oxidation Enhanced Diffusion) and TED(Transient Enhanced Diffusion)), a variety of NMOS/PMOS Transistors with different length and width are tested. After the calibration, we obtained Id-Vg profiles of NMOS/PMOS transistor with different length as shown in Fig.3. And, it is seen that I_{ON}, I_{OFF} and V_{TH} are correctly simulated on both the length of 0.3um and 20um.

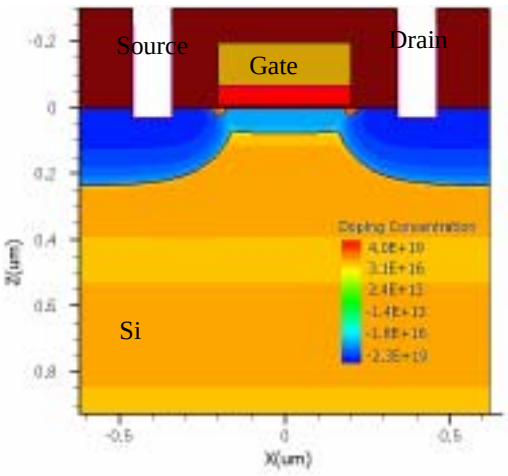

Fig.2 Doping concentration of PMOS transistor constructed by 2-D process simulation.

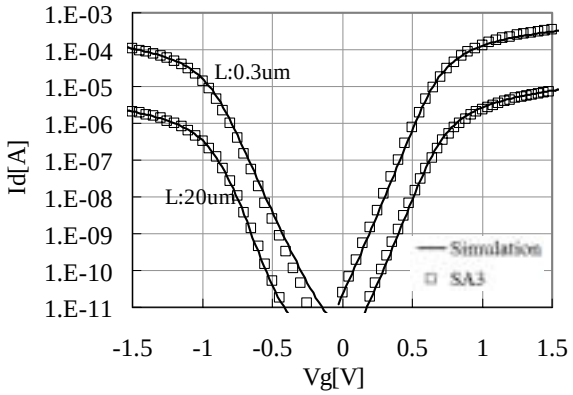

Fig.3 Id-Vg profiles of SA3(NO Annealed Gate Dielectric) sample for LVN and LVP transistor. Length dependency is shown well fitted due to the calibration of process simulation parameters.

Based on these calibration results of simulation parameter, boron concentration profile in Si is constructed as shown in Fig.4. Since the calibration is performed with typical dry oxidation models while neglecting the effect of Plasma Nitridation, we compare boron profile of SA3 sample for a start. Simulation profile shows good match to SIMS data in Si, confirming the accuracy of the calibration. The boron profile near interface shows different shape when compared to SIMS data since the material constitution near Si/SiO2 interface is different between the sample and the simulation.

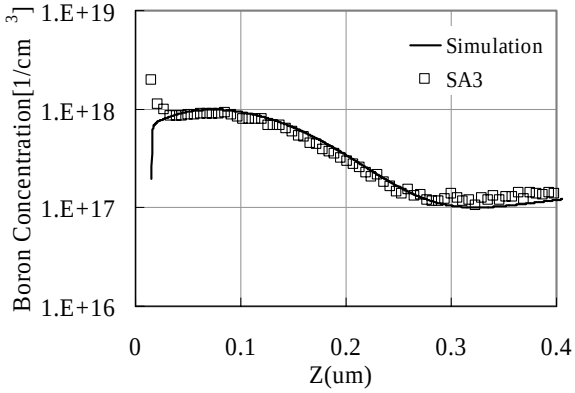

Fig.4 SIMS profile of SA3 sample and calibrated simulation result near Si/SiO_2 interface.

Fig.5 shows experimental Id-Vg curves for LVN/LVP transistor with different tunnel oxide samples. And, V_{TH} of NMOS and PMOS transistor of plasma nitrided gate oxide show 0.1V lower value than that of dry oxidation while possessing the same boron concentration. Furthermore, as shown in Fig.6 depicting C-V diagram of each sample, we observe uncommon peak near Vg=0V on buried channel PMOS capacitor with plasma nitrided gate dielectric. These results indicate that plasma nitridation evokes another issue

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in bulk SiO_2 and Si/SiO_2 surface in regardless of boron segregation in bulk Si, and it changes electrical characteristics of NMOS/PMOS transistor.

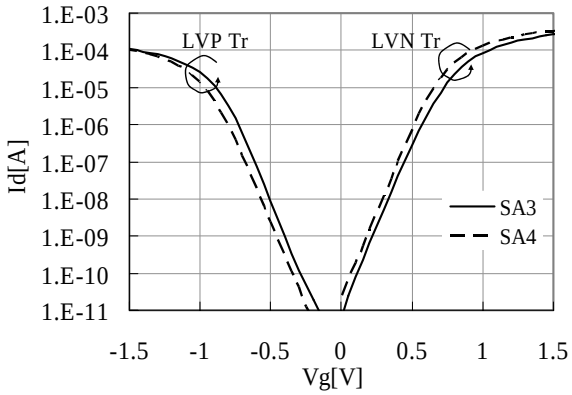

Fig.5 Id-Vg profiles for LVN and LVP transistor. SA4 sample(Plasma Nitrided Gate Dielectric) possesses 0.1V lower V_{TH} value than SA3 sample.

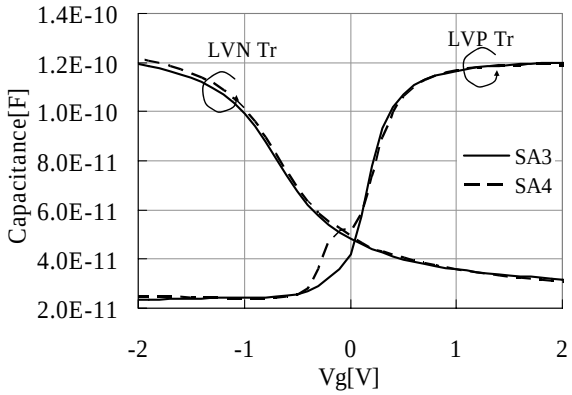

Fig.6 C-V profiles of surface channel NMOS and buried channel PMOS capacitors with different gate oxidation conditions. Buried channel PMOS capacitor of SA4 exhibits uncommon shape near Vg=0V.

2.3 C-V Diagram of Plasma Nitrided Oxide

For the purpose of identifying the reason of 0.1V difference in Id-Vg curve and abnormal peak in C-V diagram, we added several amount of oxide bulk traps and interface traps into SiO_2 and Si/SiO_2 interface deliberately, and then observed their device characteristics with 3-D simulation. As shown in Fig.7, the C-V curve is reproduced by adding excessive amount of interface trap in Si/SiO_2 interface and the amount of interface trap was measured to be 9e11 which is three times higher than that of dry oxidation. The excessive trap located near interface is regarded as the evidence of positive charge trap of the plasma nitrided gate []. The uncommon peak illustrates V_{TH} shift by electron trap/detrap of the trap sites in gate dielectric and is appeared clearly on the buried channel PMOS capacitor since its C-V curve changes under inversion condition with abundant supply of electrons from N-Well [6,7]. Whereas, surface channel NMOS capacitor shows little change owing to its change of C-V curve under the depletion condition with few electrons on Si surface. While oxide bulk trap possesses the same effect on the shift of Id-Vg curve as interface trap, it has no influence on abnormal peak of C-V diagram.

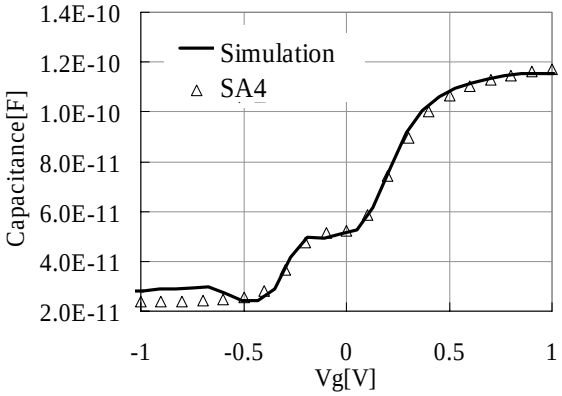

Fig.7 C-V profile for buried channel PMOS capacitor with SA4 sample and calibrated simulation result. Nit value equals 9E11 which is three times higher than that of SA3 sample.

Based on these process and device simulation parameters, Id-Vg characteristics of NMOS and PMOS transistor with plasma nitrided gate dielectric are obtained by the device simulation as shown in Fig.8. And, it shows good agreement with experimental data, confirming that 0.1V V_{TH} shift was attributed by positive charge trap of the plasma nitrided gate dielectric.

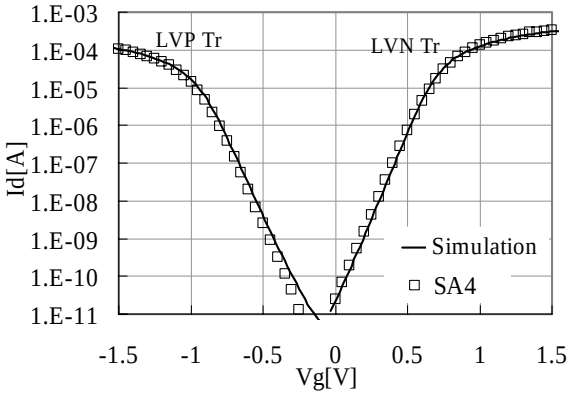

Fig.8 Id-Vg profiles for surface channel NMOS and buried channel PMOS transistor of SA4 sample. Simulation results

with N_{IT} value of 9E11 show good agreement with experiments.

CONCLUSIONS

The effect of Plasma Nitridation on the gate dielectric in terms of device characteristics is investigated through simulations and experiments. Firstly, based on accurate calibration of 3D simulation, it is verified that Plasma Nitridation has no effect on boron segregation near Si/SiO_2 interface and bulk Si. Secondly, we observe uncommon behavior of C-V diagram in the case of buried-channel PMOS transistor. And, we prove that it is due to excessive amount of interface traps generated by Plasma Nitridation.

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