A Computationally Efficient Method for Evaluating Distortion in DG MOSFETs

Ramón Salazar, Adelmo Ortiz-Conde and Francisco J. García Sánchez
Solid State Electronics Laboratory
Simón Bolívar University, Caracas 1080, Venezuela
rsalazar@usb.ve ,{ortizc, fgarcia}@ieee.org

ABSTRACT

In this work we present the use of the Integral Non-Linearity Function (INLF) to efficiently study the distortion of Double-Gate (DG) MOSFETs. Here we analyze the $I_D(V_D)$ output characteristics in the Symmetrically Driven Double-Gate (SDDG) and Independently Driven Double-Gate (IDDG) operating modes. The distortion is analyzed on Atlas simulated characteristics of an undoped-body DG MOSFET with front and back gate-oxide thickness of 2 nm and a silicon film thickness of 10 nm. Results show that 1) the Integral Non-Linearity Function (INLF) can be efficiently used to calculate IP2 and IP3, and 2) the HD_n/INLF ratio is constant under weakly nonlinear behavior. We present a simple mathematical demonstration that rigorously justifies the obtained results. It is concluded that INLF provides a computationally efficient method to calculate harmonic distortion without using Fourier or any other complex AC analysis.

Keywords: Double-Gate MOSFET, independently driven double-gate (IDDG), integral non-linearity function, harmonic distortion, IP3.

1 INTRODUCTION

CMOS has been rapidly taking on the RF market due to its continuing downscaling. Double-Gate (DG) MOSFETs operating in both Symmetrically Driven Double-Gate (SDDG) and the Independently Driven Double-Gate (IDDG) modes have shown to be useful in several relevant circuit applications [1,2]. They are expected to replace conventional bulk device because of their superior scalability [3]. One interesting application of DG MOSFETs could be as voltage-controlled linear resistor, in which the output characteristic $I_D(V_D)$ is modulated by the front (V_{GF}) and the back (V_{GB}) gate-voltages.

Distortion is a major concern in RF circuits, including voltage-controlled resistors. Several authors have addressed the analysis of distortion for DG MOSFETs [4-8]. In some cases the transfer function $I_D(V_G)$ has been studied, and in others the DG MOSFET has been analyzed as a quasi-linear resistor [4-6]. However, these studies have been done on devices with a gate oxide thickness of 30nm, a silicon thickness of about 80nm and a buried oxide of 400nm while lengths of channels varied from 4μm up to 20μm. Our aim is to study distortion in smaller devices for which some of the dimensions approach the state-of-the-art in current manufacturing processes. Specifically, we have studied the harmonic distortion in devices with front and back gate oxide thickness of 2nm, silicon thickness of 10nm and channel length of 3μm. We show the trends of distortion when varying V_{GF} in a SDDG MOSFET and when varying both V_{GF} and V_{GB} in an IDDG MOSFET.

Traditionally, distortion has been measured using different figures of merit such as total harmonic distortion (THD), *n*th-order harmonic distortion ratios (HD_n), Dynamic Range, IP2 and IP3, etc. In order to calculate any of the mentioned quantification criteria it is necessary to perform Fourier analysis to AC signals, which is a relatively complex computational operation that consumes significant amounts of time and resources.

We propose to use the INLF as an alternative criterion to quantify harmonic distortion. Calculating INLF is a much simpler than any of the operations associated with the traditional figures of merit for distortion. Our results show that under weakly nonlinear behavior, the HD_n/INLF ratio is a constant. We rigorously justify this relation by developing a simple mathematical demonstration. It indicates that for low input amplitudes the HD_n/INLF ratio is a constant which can be calculated. Therefore both criteria are equivalent as valid measures of distortion. For larger input amplitudes the ratio does not remain constant. In spite of such limitation, since the HD_n/INLF ratio can be theoretically calculated (for low amplitudes), then the INLF can be used to calculate the exact same values of IP3 or IP2 obtained by traditional methods, but without performing any tedious AC analysis. The IP2 and IP3 can be calculated using only the DC output characteristic $I_D(V_D)$ as shown in our results.

2 MATHEMATICAL RELATIONS AMONG THE INLF, HDn, IP2 AND IP3

Since 2002 a number of articles have presented the idea of using the INLF as an alternative criterion to quantify the harmonic distortion for many different applications in devices [4-8] as well as in integrated circuits [9,10]. As mentioned above, due to its relative computational simplicity the INLF represents a very attractive alternative to any of the traditional figures of merit such as THD, HD_n or IP2, since the INLF does not require calculating Fourier coefficients, Fast Fourier Transform or high-order derivatives. This is an argument common to all the authors who have studied the subject [4-10]. Aside from its computational convenience, the INLF exhibits other

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

important advantages: it reduces the noise when experimental data is processed, and it only requires to have the (analytical or experimental) *I-V* static transfer function of the device to be able to analyze its nonlinear behavior.

Although the relation between HD_n and INLF has been exploited to analyze distortion in different devices [4-10], neither the exact form of that relation, nor the extent of its validity has previously been mathematically derived. We intend to answer these questions with the simple mathematical demonstration that follows, which allows explaining the results obtained through simulations.

Let us recall the definition of INLF, frequently denoted as "*D*" [9-13]:

$$D \equiv \int_0^{I_{\max}} V\,dI - \int_0^{V_{\max}} I\,dV \quad , \tag{1}$$

where V and I are the voltage and current signals corresponding to the characteristics of the device under study, and $V_{\max}$ and $I_{\max}$ are the maximum values. A normalized expression of (1) is often denoted as "D_N" and it can be written in the following form:

$$D_N \equiv \frac{D}{V_{\max} I_{\max}} = 1 - \frac{2}{V_{\max} I_{\max}} \int_0^{V_{\max}} I dV \quad . \tag{2}$$

In general, assuming weakly nonlinear behavior, the output signal (I) would only have one dominant harmonic, say of *n*th-order. Therefore, in terms of McLaurin series, the output signal may be approximated by:

$$I \approx a_1 V + a_n V^n \quad , \tag{3}$$

a_1 and a_n being the first- and *n*th-order coefficients of the series (respectively). Since there is only one dominant harmonic, the THD is approximated to the *n*th-order harmonic distortion ratio [14]:

$$\mathrm{HD}_n = \frac{a_n}{a_1}\left(\frac{V_{\max}}{2}\right)^{n-1} \quad . \tag{4}$$

When (2) is applied to (3) and assuming that $a_1 V_{\max} >> a_n (V_{\max})^n$ the following relationship is obtained:

$$D_N \approx \frac{(n-1)}{(n+1)} \frac{a_n}{a_1} \left(V_{\max}\right)^{n-1} \quad . \tag{5}$$

Hence, the ratio between (5) and (4) is given by:

$$\frac{D_N}{\mathrm{HD}_n} = \frac{(n-1)}{(n+1)} 2^{n-1} \quad . \tag{6}$$

Therefore the D_N /HD_n ratio is a constant which depends only on *n*. This relationship holds true only as long as the amplitude of the input signal is low enough so that the total output signal can be approximated an expression with a single distortion term, such as presented in (3). Such approximation is valid for weakly nonlinear circuits, where the output power is mainly concentrated in the fundamental and the lowest-order harmonic.

When the second-order harmonic (H_2) is dominant the D_N/HD_n ratio is 2/3, which implies that D_N=2/3(H_2/H_1). In fully differential weakly nonlinear circuits where the third-order harmonic (H_3) is dominant the D_N/HD_n ratio is 2, which means that D_N=2(H_3/H_1).

When 20log(D_N) is plotted against the input-power, it will vary linearly for low input amplitudes. If this linear variation is extrapolated and intersected with either 20log(2/3) (H_2 dominant) or 20log(2) (H_3 dominant), the resulting intersection would be the point for which H_2=H_1 or H_3=H_1 respectively. In other words, this method exactly produces the IP2 and IP3 input intersect points. Therefore, regardless of the amplitude of the input signal, D_N can be used to calculate the exact values of iIP2 and iIP3 for any kind of device (or circuit), but without having to perform any AC analysis.

3 RESULTS AND DISCUSSIONS

In this section we present the results obtained through simulations using Atlas version 3.18.1R from Silvaco. The studied device is an undoped-body DG MOSFET with front and back gate-oxide thickness of 2 nm, a silicon film thickness of 10 nm and a channel length of 3μm. The device was operated in both the SDDG and IDDG modes and the $I_D(V_D)$ output characteristics was analyzed.

Figure 1 shows the dependence of the D_N/THD ratio on V_D at different V_{GF} values. It can be seen that for low input amplitudes (below 5mV) the D_N/THD ratio is constant and approximately equal to 0.67. This is in agreement with equation (6). Since the device is operated in the triode region, $I_D(V_D)$ should exhibit a behavior that tends to a quadratic dependence, and therefore H_2 should be the dominant harmonic.

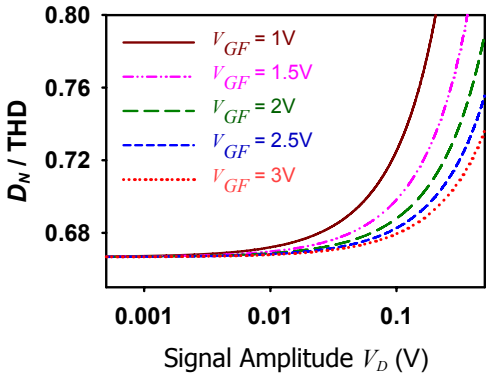

Fig. 1. D_N/THD vs. V_D for the SDDG MOSFET at different V_{GF}.

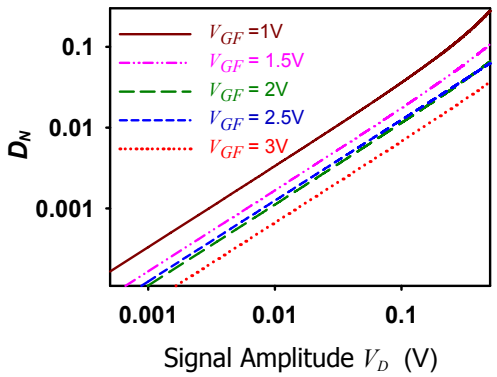

Fig. 2. D_N vs. V_D for the SDDG MOSFET at different V_{GF}.

According to (6) if H_2 is dominant the D_N/HD$_n$ ratio is 2/3 (as seen in Figure 1). For larger input amplitudes this relation is no longer valid and the D_N/THD exhibits a strong nonlinear dependence on V_D.

Notice in Figure 1 that for high V_{GF} values, it takes larger input amplitudes to make the D_N/THD ratio deviate from its constant value of 2/3. Since this deviation occurs when higher-order harmonics become significant in the output signal, this implies that high V_{GF} values make the device more linear. This statement is confirmed by the results shown in Figure 2, where we plotted the variation of D_N as a function of V_D. In Figure 2 it is seen that the distortion increases when increasing V_D but decreases when augmenting V_{GF}.

The fact that all the curves in Figure 2 have approximately the same slope implies that V_{GF} does not modify the power-law dependence of D_N on V_D. Notice also that for V_D greater than 10mV, D_N keeps increasing at the same rate, which reflects an increasing distortion. However, that does not mean that above 10mV the relation between D_N and THD is still a constant.

Figure 3 shows plotted separately THD and D_N as a function of V_{GF} for different V_D at which the D_N/THD ratio is not constant. It can be seen that even though the relation between the two distortion criteria is not the same, the trends are remarkably similar and therefore D_N still represents a measure of distortion.

In order to prove that D_N can be used to calculate the iIP2, we processed the data from simulations and calculated H_1 and H_2 (Fourier's coefficients) to obtain the iIP2. Then, we applied the new method described in section 2 and compared both (the traditional and the proposed new procedure) for different V_{GF} values. In all cases the calculated iIP2 was the same regardless of the method used.

Figure 4 shows a particular example at V_{GF}=1V. Figure 4*a* shows the iIP2 obtained through the classical procedure and Figure 4*b* shows the iIP2 calculated with D_N. It can be seen that the iIP2 is the same in both cases, only that to obtain Figure 4*a* Fourier analysis was required, whereas the $I_D(V_D)$ output characteristic was enough to calculate the iIP2 shown in Figure 4*b*.

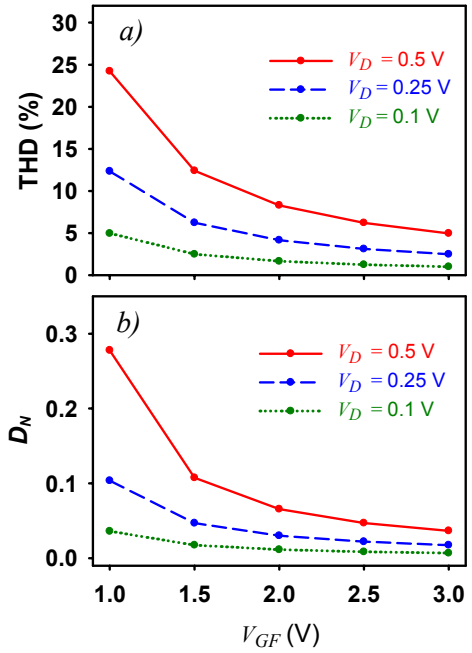

Fig. 3. *a)* THD vs. V_{GF} and *b)* D_N vs. V_{GF} for the SDDG MOSFET at different V_D.

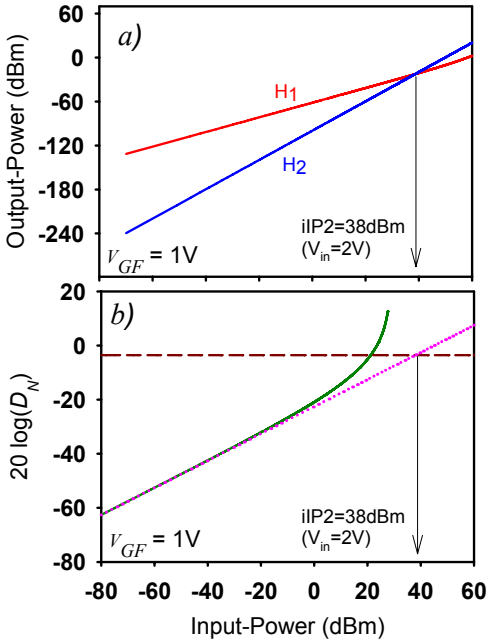

Fig. 4. Nonlinear characteristics of the SDDG MOSFET. *a*) Conventional diagram for iIP2 calculation. *b*) Present method for iIP2 calculation (no AC analysis is required). The solid line is the variation of D_N respect to the input, the dotted line is the extrapolation of the linear behavior of D_N . The dashed line is 20log(2/3) i.e. 20log(D_N) at H_1=H_2. The Input-Power is referred to a 50Ω resistor.

Figure 5 presents the trend of iIP2 for varying V_{GF} values in the SDDG MOSFET. It can be seen that for an increase in V_{GF} from 1V to 3V the iIP2 has an increase of about 30 dBm, which is a considerable improvement in linearity.

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

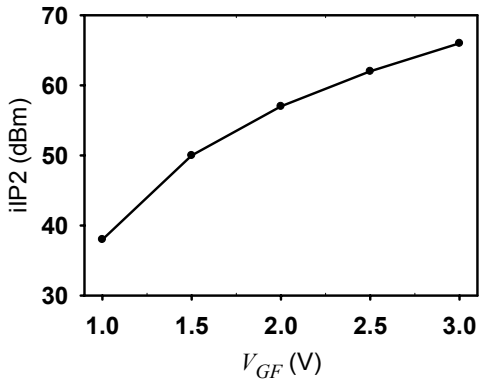

Fig. 5. iIP2 vs. V_{GF} for the SDDG MOSFET.

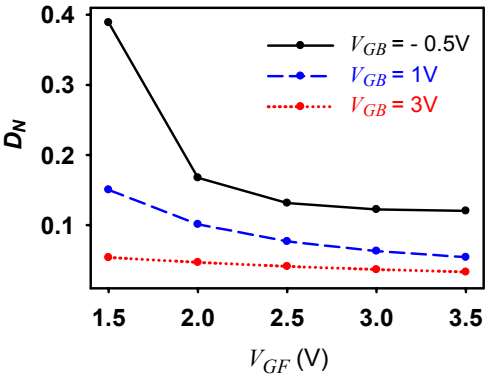

Fig. 6. D_N vs. V_{GF} for IDDG MOSFETat three different V_{GB} with V_D= 0.5V.

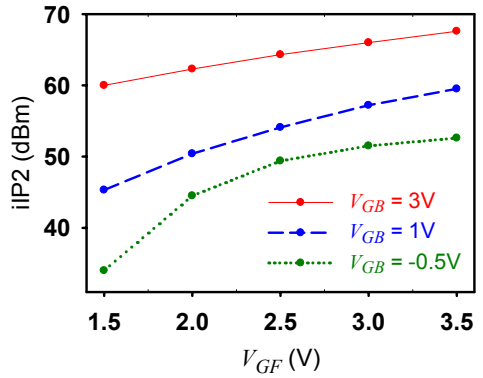

Fig. 7. iIP2 vs. V_{GF} for the IDDG MOSFET at three V_{GB}.

The trend of distortion in Figure 5 is consistent with the trend observed in Figure 3.

Figure 6 shows the variation of D_N of an IDDG MOSFET as a function of V_{GF} at different V_{GB} values for a fixed V_D of 0.5V. It is clear from Figure 6 that increasing V_{GF} as well as V_{GB} contributes to improve the linearity of the device's output characteristics.

Figure 7 presents the variation of iIP2 with respect to V_{GF} for the IDDG MOSFET, using the proposed new method. It is seen that it is consistent with the trend of D_N observed in Figure 6. Notice that increasing V_{GB} improves the linearity of the device and it also makes the distortion less sensitive to changes in V_{GF}.

4 CONCLUSIONS

We have proposed a new method for calculating iIP2 and iIP3 based only on the device's characteristics. The new method produces the same results as traditional procedures, but without having to perform Fourier or any other kind of AC analysis. The new method thus allows a quick and efficient computation of distortion for any kind of device or circuit.

We have mathematically demonstrated that for devices exhibiting weakly nonlinear behavior the D_N/HD$_n$ ratio is a constant which can be theoretically calculated. These conclusions were confirmed by the results obtained from simulations. Although the D_N/HD$_n$ ratio is constant only for low input amplitudes, D_N still represents a measure of distortion for relatively high input amplitudes.

The proposed new method was applied to simulated $I_D(V_D)$ output characteristic of a DG MOSFET operated in SDDG and IDDG modes. The analysis of distortion derived from $I_D(V_D)$ indicates that regardless of the operation mode, the increase of V_{GF} always improves the linearity of the output characteristic. In the case of the SDDG MOSFET the distortion increases as V_D is increased, whereas in the case of the IDDG MOSFET the distortion is diminished by increasing V_{GB}.

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