THE LOGIC ELEMENTS "AND"/ "OR" ARE ESTABLISHED ON THE ELEMENTS WITH PUNCHTHROUGH AND DEFORMATION SPACE CHARGE REGIONS

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ABSTRACT

The punchthrough (PT) effect, which occurs in different semiconductor devices, was described as a parasitic phenomenon during engagement of top and bottom gates of Junction Field Effect Transistors (JFET)s. For a long period of time the PT had been looked at as an unwished nonoperating process with leakage and low breakdown voltages.

We developed new devices based on the punchthrough (PT) effect, which spited in three groups: the current's (CPT), the voltage's (VPT), and the opposite (OPT) processes. New logic elements are discussed as a conceptual idea.

Keywords: design, effect, logic elements, punchthrough, punch-off, reachthrough

1 INTRODUCTION

The punchthrough (PT) effect, which occurs in different semiconductor devices, was described as a parasitic phenomenon during engagement of top and bottom gates of Junction Field Effect Transistors (JFET)s. For a long period of time the PT had been looked at as an unwished nonoperating process with leakage and low breakdown voltages. J. Lohstroh and J.M. Shannon [1, 2] started widely applying the PT structures in different devices with various features of the punchthrough effect [3-6].

2 THREE GROUPS OF THE PT DEVICES

Various semiconductor structures, which are used widely as PNP (NPN) – transistor sandwich design, use only one word "punchthrough" to describe the PT effects. We suggest splitting all of them in three different groups: the punchthrough effect or the current's punchthrough (CPT) effect; a reachthrough or the voltage's punchthrough (VPT) effect; and punch-off or the opposite punchthrough (OPT) effect. The common condition for all noted above devices is the fully depleted middle layer by the mobile carriers, N (P) –type's conductivity. They have a different schemas of connection: the floating base (FB), the short-cut (SC) - with middle layer - injecting (emitter – in the bipolar structures) PN - junction for the CPT mode; the "floating" body (FBOD) for the VPT process; and reverse-bias voltage on the both PN - junctions for the OPT condition. At the moment of touching of space charge regions both P+N – junctions in the middle layers of all three groups have the common condition – depleted central layers, but it is only true for the moment when they touch. The behavior of all the devices in the groups changes completely after any increment in the voltage which applies in the structures with different types of the PT processes - Fig. 1 (a, b, c, d). For the description we will use the first PN – junction as an emitter, the other one – as a collector.

Reduction ($\varphi ce - Ue$) of the height of the potential barrier - φce of the SC's PN – junction or the same emitter junction for the FB scheme (Fig. 1 a, b) occurs in the CPT, where Ue – forward drop voltage on the emitter junction.

For the VPT process the potential of the floating P (N) – region of the emitter PN - junction starts repeating the potential of the collector junction and the emitter drop voltage will be determine as:

$$Ue = \varphi ce + Uc - Ucpto, \quad (1)$$

where: Uc – drop voltage on the collector's junction;

Ucpto – punchthrough voltage for the FBOD scheme (the reachthrough condition – Fig 1c).

The opposite PT process with the punch-off (pinch-off) or Upt-off voltage is shown on the Fig. 1d. The space charge regions of the both pn – junctions start increasing their sizes with the deformation of their shapes (on the both PN– junctions are applied the same reverse-bias voltage – Uer. The structures based on the PT effect develop very fast for the last ten years. The Patent Agency of the U.S.A. introduced four new chapters for this type of devices in 1999. One of the main areas with the largest acceleration in research and technical solutions is ESD, protection and low voltage's stabilitrons (Zener) diode [3, 6}. The various structures: N+PN+ (P+NP+), N+PP+N+ are employed with the both SC and FB schemas in the CPT mode. For stabilitrons of the variable operating voltages the principles, described in "THE INITIAL REVERSE-BIAS INJECTING P+-N JUNCTION MODE IN P+-N-P+- STRUCTURES WITH PUNCHTHROUGH" (see article in Proceeds Nanotech 2007) can be used. New possibility provides the method of thermal compensation and various stabilitrons,

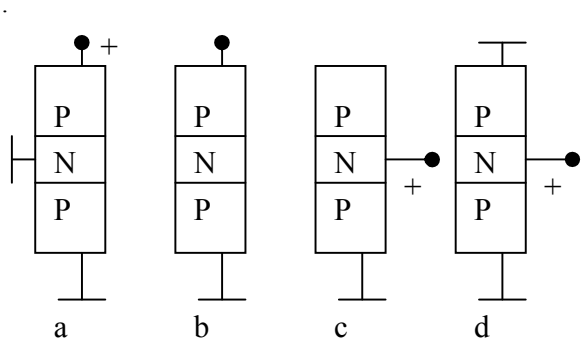

Fig.1 (a, b, c, d) Connection of PNP (NPN) – structures with various punchthrough processes:

a. The short-cut emitter PN – junction in the current's punchthrough mode;

b. The floating-base connection in the current's punchthrough mode;

c. The scheme with the voltage's punchthrough mode;

d. Connection for the opposite's punchthrough devices

based on this solution [7]. The method based on the alignment of the avalanche or Zener's breakdown and has two PT processes with the transformation into each other. The design is shown in the Figure 2.

The VPT process occurs in the moment when the SCRs of p-n and p+-n – junctions touch each other As the result the p+ - region potential would be described in Eq. (1).

As the voltage Uca continues increasing the critical electric intensity on the p+-n+ - junction provokes its avalanche or thermal emission (Zener's) breakdown.

The current in the structure has avalanche characteristic (not diode's one). The several designs of stabilizing diodes based on this method have been researched in [8]. The PT process has a negative temperature coefficient; avalanche breakdown has a positive one and Zener's (thermal emission) effect has a negative temperature coefficient as well. This method allows for designing of Zener diodes and manipulating temperature coefficient over the range (minus; ≈ O; plus). In this P+NP+N+ - structure two features of the PT effect are combined with the avalanche breakdown: 1. the VPT process which is described by Eq. (1) before breakdown; 2. the CPT in which the VPT was transformed after the breakdown. In the [9] a peculiar field punchthrough mode was studied by regarding the structure to be composed of two transistor subsystems coupled by a field domain in the semiconductor p+-p--n-p+-n++ structures. This kind of multilayered structures without p-layer transforms into stabilitron [7], as a particular case.

3 PT TYPES OF OPERATING ELEMENTS FOR LIQUID CRYSTALL DEVICES

The first thin film transistor (TFT) was designed in1979. That time it was an exotic thing to be used widely

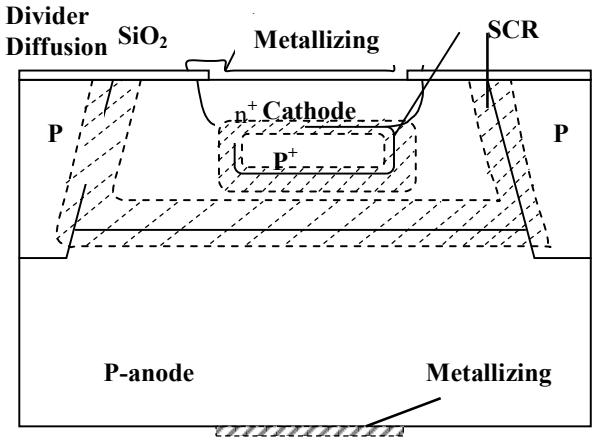

Fig.2 The thermal compensated stabilitron (Zener) diode [8]

in the semiconductors. On the other hand fast development liquid crystal devices (LCD) required designing new active operating elements for LCDs. The results of research of J.M. Shannon and J Lohstroh in various areas of application of the PT effect showed a perspective a new "phenomenon" in this employment.

These types of operating elements for LCD were developed in [8]. The analog indicator [10] includes analog-digital converter (ADC) is manufactured on the Si – wafer. It contains high resistance substrate n – type in which formed the busbar and indicators' elements p+ - conduction, Fig. 3 The lengths between busbar and elements have to fulfill the condition to provide the VPT process between SCRs of the busbar and indicators' elements. By variation of lengths, we can obtain linear, logarithmic or back logarithmic dependences. The standard technology allows quite easy to carry out lateral or vertical structures.

The matrix LCD [11] is established on the same principle like a TV screen [12]. It allows excluding constant component of current in these devices that is why growing long term and reliability LCD is. The solution [12] has increased reliability by applying protection over voltage's element which formed simultaneously with other active elements of LCD. The VPT and the CPT processes are combined in this matrix liquid crystal device. The VPT is usual operating mode, The CPT is the over voltage's mode. The work principle of these "high resistance switchers" P+NP+ - structures [10-13] is based on the VPT. In [14] was suggested term "A "floating" analog voltage switchers" for these types of the structures with the VPT operating method. After reachthrough voltage, the indicator's element potential becomes higher. As result, the respective LCD element afterwards gets threshold voltage for liquid crystal material and becomes visible. . The VPT and the CPT processes are combined in the matrix liquid crystal device [13]. The VPT is usual operating mode. The CPT is the over voltage's process. The various technical solutions [15 - 18] utilize PNP (NPN) – structures with the PT in the active

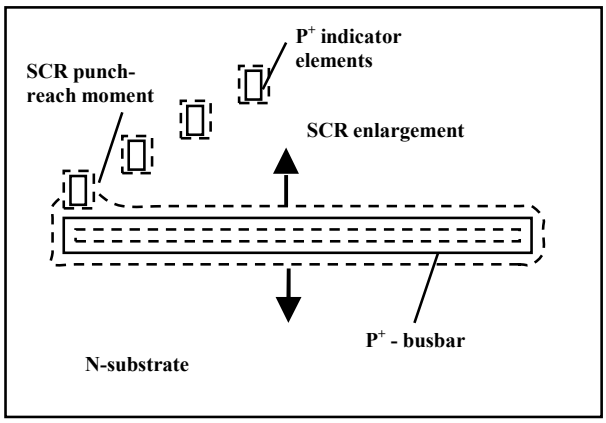

Fig.3 The Analog – digital converter performed with lateral P+NP+ - structures in the voltage's punchthrough mode (the semiconductor part) of the analog indicator [13]

matrix displays and TV screens.

4 PT PROCESSES IN FETS

JFETs gave start for development of devices with the various PT modes. The punch-off (pinch–off) voltage – Up.off is the usual state-off condition for closed JFETs. The gate operating voltage – Ug in this case higher then Up.off: |Ug| - |Up.off| < 0. In the present time appeared the different FETs: DEPFET [19], FOXFET [20], PT FET [4], Four-Gate Transistor [21], four-terminal JFET [1, 22], some transistors for special purpose [23-25], etc. All of them apply not only the OPT as conventional mode of operating but combine with at least one more the PT mode.

The DEPFET [192] utilizes the VPT for the non-destructive readout and reset. This depleted JFET has separated top and floating bottom gate and the method operation with principals the voltage's punchthrough process, which was described in [1].

In the silicon strip detectors [20] strips are biased from common P+ - diffused bias line through an undiffused gap region (n – channel in MOS – transistor), controlled with the gate-field-induced effect. Such the gated PT biasing structure is also known as a field –oxide field effect transistor (FOXFET). In this device utilizes the VPT and fully depletion the middle n- layer in the detector area. This kind of the MOS transistor is really the PT MOSFET.

The PT FET [4] combines the MOS transistor and the CPT bipolar transistor with the SC emitter - base P+N – junction.

The four-gate FET [21] mixes MOS and JFET with double the OPT.

The four-terminal JFET [19] can be used with the grounded, floating and reverse-bias bottom gate and operated in the SC and FB schemas in the CPT and the VPT modes.

The long-tailed JFETs [23, 24] are full analog long-tailed pair triodes, which A. Blumlein patented in 1936. Long-tailed JFETs (with extended VAC - analog "varimu" valves) are used as voltage comparators, the input stages of operational amplifiers, and other circuitry where their nearly infinite gate impedances can reduce the loading upon preceding circuitry. The input VAC has two parts: slope- II and abrupt - I. The both solutions [23, 24] performed as the parallel connection of the two JFETs with different transconductances and punch-off voltages. The solution [24] allows limiting the PT current (the CPT process) after the bottom and top gate's engagement (overvoltage mode) by employing variable resistor between source and the part of the top gate.

The JFET with built-into protection [25] design has fulfilled like a functional integrated device where combined the PT PNP - bipolar transistor and n-channel JFET. The PNP - structure optimized to get minimum leakage in the PT structures before their operating. The protection devices works in mode with the SC emitter junction and provides leakage before the CPT process close to 2 orders (100 times) less than the same structures but with the FB schemas [26].By introducing this type of protection, practically, 1/F- noise level is not affected.

5 LOGIC ELEMENTS "AND"/"OR"

We suggest to discus as a concept logic elements "AND"/"OR" based on the CPT effect and deformation (element "AND") of SCRs.

1. On the substrate N- type is formed lateral P+ - bodies 1 – injector and 2 – operating elements. By supplying a negative voltage equal to the CPT voltage (U_{cpt}) on one element 2 is occurred the CPT process of SCRs into P+-N-P+ - structure (injector -1 through load resistor is grounded terminal). After the CPT effect in the device is appeared through current and on the load resistor is assigned a signal. The same process is repeated with other operating element – 2. We have logic operation "OR".

The length d1 is defined from two conditions:

$$d1 < d2 \; ; \; d2 \geq 2\sqrt{2}\varepsilon\varepsilon o(\varphi c + U_{cpt})/qN_D, \qquad (2)$$

where: d1 – length of the gap between ihjector and operating elements;
d2 – length of the gap between two neighboring operating elements;
N_D – the concentration of the donor purity in the substrate;
εo, ε – the permittivity of vacuum and relative permittivity of the semiconductor, respectively.

In this case operating signals of elements –2 do not interact between itself.

2. Lengths: d1 and d2 are changed in logical element

$$\text{"AND": } d1 > d2; \; d2 \leq 2\sqrt{2}\varepsilon\varepsilon o(\varphi c + U_{cpt})/q\, N_D \qquad (3)$$

By supplying only one the operating signal - U_{cpt} to the element – 2, the CPT process is not occurred between bodies 1 and 2, so d1 > d2.

By applying two negative operating signals simultaneously is happened punch – off state, the OPT process with engaged elements – 2. So d1>d2, deformation of their SCRs started. The both deformed SCRs extend faster in the direction, which perpendicular of the gap between two neighboring operating elements and get the SCR of the injector-substrate pn – junction. The CPT process gets beginning and on the load resistor is allocated a signal. This is logical element "OR".

6 CONCLUSION

We discussed the some devices with different operating modes and various connecting schemas in the CPT, the VPT, and the OPT processes The PT structures continue development with new features: in physical processes "…field punch-through mode" [9]; in original methods of operating of the PT devices "... double punchthrough" [1] and of combined structures [27]. The PT FETs [4] had to be improved design parameters in MOSFET by applying the SC schema in the CPT bipolar transistor and a new method of operating [27] for this kind of PT FETs.

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