Modeling of Saturation-Region Characteristics of Nanoscale Double-Gate MOSFETs

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ABSTRACT

Nanoscale double-gate (DG) MOSFETs, e.g., FinFETs, are significantly different from their conventional single-gate counterparts, i.e., bulk-Si and PD/SOI MOSFETs. For example, the viable DG MOSFET has an undoped ultra-thin body (UTB with thickness t_{Si}) between the two gates, which results in unusually low transverse electric field and quite high carrier mobility (μ_{eff}) [1], [2]. These features produce significant saturation-region effects that are not prevalent in the conventional devices, or/and have not been modeled well conventionally. In this paper, we discuss these effects and how they are accounted for in our physics-based compact model UFDG [3].

Keywords: Physical compact model, FinFET, velocity overshoot, DIBL/DICE.

1. CARRIER VELOCITY OVERSHOOT

In conventional nanoscale MOSFETs, the saturation region, indicated by channel-current saturation (at $I_{DS(sat)}$), is usually defined by carrier velocity saturation (at $v_{sat} \cong 10^7$cm/s) at $V_{DS} = V_{DS(sat)}$ well below that required to pinch-off the (gradual) channel. However, in the undoped DG MOSFET, the noted high μ_{eff} can cause significant velocity overshoot, which increases $V_{DS(sat)}$ and $I_{DS(sat)}$. The velocity overshoot in UFDG is modeled [4] based on carrier temperature ($T_c > T$), which "lags" the longitudinal electric field E_y along the channel. (An empirical model based only on E_y is unreliable.) The T_c-based modeling is derived from the first and second moments of the Boltzmann transport equation in the channel, appropriately simplified to

$$v = \mu_{eff}(E_y)E_y\left(1 + \frac{k_B}{qE_y}\frac{dT_c}{dy}\right) \qquad (1)$$

and

$$\frac{d}{dy}(T_c(y) - T) + \frac{(T_c(y) - T)}{(5v\tau_w/3)} = \frac{2qE_y(y)}{5k_B}\ , \qquad (2)$$

where τ_w is the energy relaxation time and v is the average carrier velocity. Combination of (1) and (2) relates T_c to E_y, and characterizes v(y), including overshoot as reflected in (1). A universal representation of the steady-state $\mu_{eff}(E_y)$ [5] enables the needed characterization of τ_w. The needed $E_y(y)$ is taken from the basic channel-current modeling in UFDG, which has been recently upgraded as overviewed in the next section.

The derived characterization of v(y) is not directly useful in a compact model. We thus use it to define a spatially independent, bias-dependent effective $v_{sat(eff)} > v_{sat}$ to replace v_{sat} in the channel-current formalism. The onset of saturation is thus delayed, and $V_{DS(sat)}$ and $I_{DS(sat)}$ are properly increased, in accord with the velocity overshoot. The modeled transport becomes quasi-ballistic, while the basic UFDG formalism is maintained. We define $v_{sat(eff)}$ based on an average transit time in the modulated portion of the channel, $\Delta L = L_{ch} - L_{gch}$ as defined in the next section:

$$v_{sat(eff)} = \Delta L\left[\int_{\Delta L}\frac{1}{v(y)}dy\right]^{-1}\ . \qquad (3)$$

We note that the ballistic-limit current is accounted for in UFDG by limiting $I_{DS(sat)}$, modeled with $v_{sat(eff)}$, based on the thermal injection velocity in the discretized 2-D-carrier energy subbands defined by the quantization modeling [2].

UFDG simulations of nanoscale DG MOSFETs imply the significance of velocity overshoot. The predicted I_{DS}-V_{DS} characteristics for an undoped 18nm n-channel device, with and without overshoot, shown in Fig. 1 exemplify the current enhancement, although it is restricted some here because the currents are near-ballistic [2]. We stress that the degree of overshoot correlates with the high electron mobility; less hole velocity overshoot is predicted for pMOSFETs. In fact, $v_{sat(eff)}$ decreases with increasing V_{GS} due to mobility degradation [4], but that is obviously not a predominant effect in the DG MOSFET of Fig. 1.

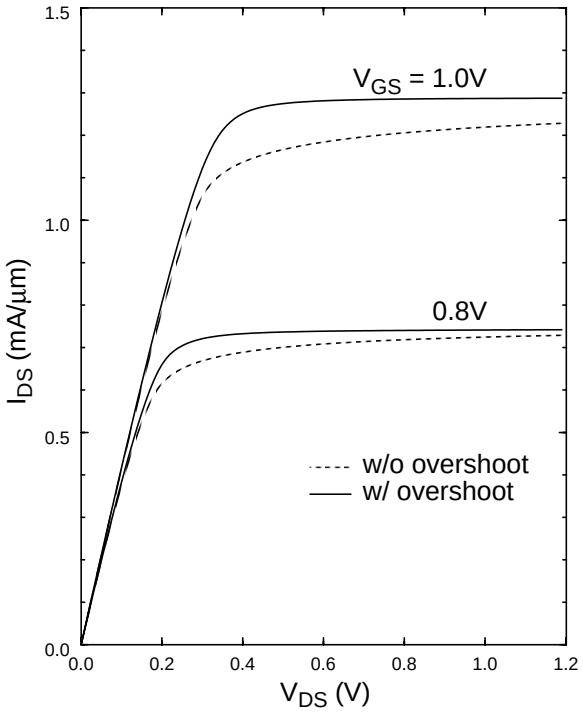

Fig. 1. UFDG-predicted current-voltage characteristics of an undoped L_{gate} = 18nm n-channel DG MOSFET, with and without velocity overshoot; midgap gate, t_{ox} = 1.0nm, t_{Si} = 9nm.

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2. DICE

Calibrations of UFDG to fabricated nanoscale DG FinFETs have tended to give results like the I_{DS}-V_{GS} characteristics shown in Fig. 2. Note that the predictions agree well with the measured data at low V_{DS}, but not at high V_{DS}, i.e., in the saturation region where UFDG underpredicts $I_{DS(sat)}$. We have inferred from such results for nanoscale DG MOSFETs, complemented by numerical device simulations, that "DICE" (drain-induced charge enhancement, which is a strong-inversion counterpart to DIBL in weak inversion [7]) can significantly affect the saturation-region current and capacitance characteristics. This effect is also promoted by the high μ_{eff}.

The saturation region of the nanoscale MOSFET is characterized by a channel that can be divided into a gradual portion ($0 < y < L_{gch}$) adjacent to the source, and a high-E_y portion ($L_{gch} < y < L_{ch}$) adjacent to the drain in which $v \cong v_{sat(eff)}$ for a given bias ($V_{GS} > V_t$ and $V_{DS} > V_{DS(sat)}$). DICE is manifested as a nearly uniform increase in the inversion-charge density (ΔQ_{ch}) along the entire channel, increasing $I_{DS(sat)}$. Furthermore, it is quite significant in defining L_{gch} and the gate capacitance; without DICE, the common (2-D Gauss law-based) analysis of the high-E_y portion of the channel [7] is erroneous, predicting that L_{gch} goes to zero prematurely, i.e., that the carrier velocity tends to saturate along the entire channel.

We model DICE via an approximate solution of the 2-D Poisson equation in the rectangular UTB/gradual channel of a generic DG MOSFET. Accounting for bulk inversion, which is quite significant in DG MOSFETs with undoped UTBs [8], we derive

$$\Delta Q_{ch} \cong -\varepsilon_{Si} t_{Si} \frac{2V_{DS(eff)}}{L_{gch}^2} , \qquad (4)$$

where $V_{DS(eff)}$ ($\cong V_{DS(sat)}$) is the effective bias at the end of the gradual channel. A 2-D characterization of the high-E_y portion of the channel, based on Gauss's law as in [7] but now including ΔQ_{ch}, defines L_{gch} in terms of $V_{DS(eff)}$, and the UFDG channel-current analysis defines $V_{DS(eff)}$ in terms of L_{gch}. These two relations are solved simultaneously using Newton-Raphson iteration. Longer L_{gch} is predicted, relative to that predicted without DICE, in accord with numerical-simulation results. This difference, as well as all DICE effects, tend to become more prevalent as L_{gate} is scaled, as implied by (4). The previous UFDG formalism, without ΔQ_{ch}, is then directly upgraded for DICE by adding (4) to $Q_{ch}(y)$. The channel current is thereby enhanced, and the terminal charge modeling, and all the capacitances and transcapacitances thereby defined, are modified accordingly.

We include in Fig. 2 upgraded-UFDG prediction of the I_{DS}-V_{GS} characteristics for the undoped 60nm p-channel DG FinFET. Note the model-data agreement now at high V_{DS}, which shows that DICE increases the on-state current by about 7%. The enhancement is more dramatic in DG devices with shorter L_{gate}. For the 18nm device of Fig. 1, the high-V_{DS} current is near ballistic [2], and is increased by almost 30% directly by ΔQ_{ch}. Further, because DICE moderates L_{gch} as noted above, the upgraded UFDG-predicted gate capacitance characteristic at high V_{DS} for this device is much better behaved, and in accord with numerical simulations. Indeed, DICE is an important mechanism in nanoscale DG MOSFETs because of this refinement as well as the current enhancement. It must be included in physics-based compact models for such devices.

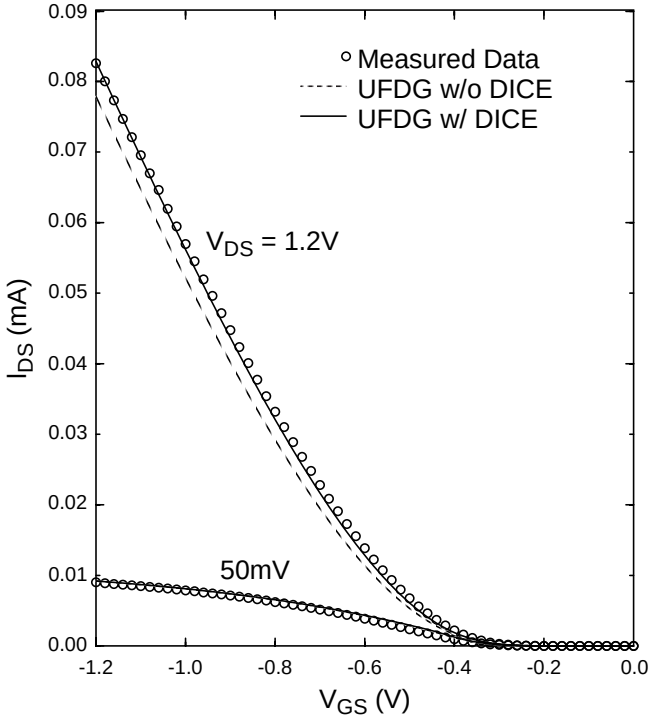

Fig. 2. Results of calibrating UFDG to an undoped L_{gate} = 60nm p-channel DG FinFET [6], with and without DICE; near-midgap gate, t_{ox} = 1.5nm, fin aspect ratio is 100nm/17nm (t_{Si} = 17nm).

ACKNOWLEDGMENT

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