Mechanical Properties Measurements of 0.35-µm BiCMOS MEMS Structures

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ABSTRACT

CMOS-MEMS mechanical properties, such as effective Young's modulus, axial residual stress, and vertical and lateral stress gradients, are strongly dependent on composition, i.e., relative metal and dielectric content. Test structures, measurements and FEA simulations are reported on these four mechanical properties for high-aspect-ratio (HAR) MEMS structures with different compositions, formed by post-CMOS micromachining of two different 0.35-µm BiCMOS technologies provided by Jazz Semiconductor and STMicroelecronics. FEA simulation results verify the experimentally extracted values of effective Young's modulus and axial residual stress. Die-to-die effective Young's modulus variations are 2 GPa for Jazz chips and 3 GPa for ST chips. Variations of axial residual stress, and vertical and lateral stress gradients are strongly dependent on post-CMOS processing.

1 INTRODUCTION

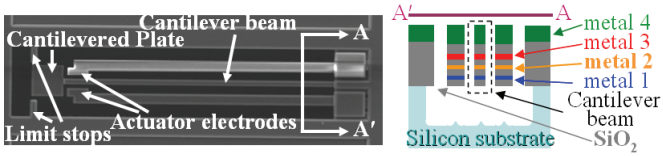
Mechanical properties characterization of MEMS structures is increasingly important in view of improving reliability and decreasing the design cycle time of new MEMS devices. Building MEMS devices based on CMOS processing has many advantages. CMOS fabrication is fast, reliable, repeatable, economical, and available through external foundries, thus decreasing the size and cost, and improving the productivity and reproducibility of MEMS devices [1]. Most importantly, integration of the high-performance electronics with MEMS structures involves only incremental processing after CMOS processing is completed, thus enabling a shift in research focus from processing details to the design and integration of complex systems with multiple sensors and actuators on a single chip. Several kinds of CMOS-MEMS technologies have been developed to meet a variety of application needs [2-6]. Several universities and institutes are working toward standardized CMOS-MEMS processing [4-6].

In this paper, we present mechanical properties measurements of high-aspect-ratio 0.35-µm CMOS-MEMS structures with different compositions.

2 EXPERIMENTAL MEASUREMENT

2.1 Effective Young's Modulus

Homogenous cantilever beam resonators are usually used in measuring effective Young's modulus of MEMS materials [1] [7]. A cantilevered plate resonator (Fig. 1) has been designed and used in our lab to measure effective Young's modulus for CMOS-MEMS metal/dielectric structures. Effective mass theory has been used in modeling the resonator. The plate provides the ability to test influence of plate size and/or composition on resonant frequency, so that density of metal/dielectric may be also extracted.



(a) (b)

Fig.1. (a) A cantilevered plate resonator, and (b) cross section of a m1-2-3-4 resonator

The analytical equation for resonant frequency of the cantilevered plate resonator is expressed in Eq. 1, where L_b is the (cantilever) beam length, L_p is the (cantilevered) plate length, E is the effective Young's modulus, H_b is the beam height, W_b is the beam width, m_{Lb} is the mass per unit length of the beam, and m_{Lp} is the mass per unit length of the plate. Metal density of 2700 kg/m^3 (for m1, 2, 3 and 4) and SiO_2 density of 2200 kg/m^3 are used in calculating m_{Lb} and m_{Lp}. Electrostatic spring softening is very small and negligible.

Cantilevered plate resonators with different compositions manufactured using the Jazz and ST 0.35-µm BiCMOS processes [8-9] have been tested. The actual dimensions of the resonator cross-sections were measured from scanning electron microscope (SEM) images. Table 1 and 2 summarize the results, where the columns filled with "●" show the layer composition, the "$\bar{E}$/SD" column shows the average effective Young's modulus and standard deviation (SD) of measurement results from three CMOS-MEMS chips manufactured in the same (BiCMOS) run, and the "*volume*" column shows the volume ratio of metal and dielectric of the beam. Die-to-die variations are about 2 GPa for Jazz chips and 3 GPa for ST chips.

Let us assume that the measurement error of f_r is 500 Hz, H_b is 10 nm, W_b is 10 nm, L_p is 10 nm, m_{Lb} is 10 kg/m^3, and m_{Lp} is 10 kg/m^3, at f_r = 74.5 KHz, the nominal E is 61.9 GPa for a Jazz m1-2-3-4 resonator with field oxide, and the estimated E error is 1.6 GPa.

$$f_r = \frac{\sqrt{35}}{2\pi}\sqrt{\frac{EW_b{}^3H_b(4L_b{}^2+6L_bL_p+3L_p{}^2)}{\{m_{Lb}L_b{}^3(132L_b{}^2+182L_bL_p+63L_p{}^2)+35m_{Lp}L_p(16L_b{}^4+48L_b{}^3L_p+63L_b{}^2L_p{}^2+42L_bL_p{}^3+12L_p{}^4)\}}} \quad (1)$$

m4	m3	m2	m1	po	fo	Ē/SD(GPa)	volume
•	•	•	•		•	61.6/0.47	1.09:1
•	•	•	•			61.6/0.48	1.05:1
	•	•	•		•	59.6/0.94	1.64:1
	•	•	•			56.8/0.77	1.54:1
		•	•		•	52.7/0.43	1.71:1
		•	•			48.9/0.80	1.56:1
			•		•	51.9/0.43	1.92:1
			•			51.2/0.84	1.61:1

Table 1. Effective Young's modulus measurement results from Jazz CMOS-MEMS (po = polysilicon, fo = field oxide)

m5	M4	m3	m2	m1	po	fo	Ē/SD(GPa)	volume
•	•	•	•	•		•	64.3/0.57	1.01:1
•	•	•	•	•			66.6/0.58	0.94:1
	•	•	•	•		•	68.2/1.09	1.68:1
	•	•	•	•			69.6/1.26	1.53:1
		•	•	•		•	76.2/0.69	1.76:1
		•	•	•			76.7/1.19	1.55:1
			•	•		•	93.9/0.84	1.91:1
			•	•			95.3/1.03	1.60:1

Table 2. Effective Young's modulus measurement results from ST CMOS-MEMS

2.2 Axial Residual Stress

Owing to high temperature in CMOS processing, such as deposition, thermal oxidation, etc., each layer may be compressive or tensile. Axial residual stress in the layers gives rise to vertical and lateral curling effects. Vertical and lateral stress gradients of the composite beam arise from the combination of layer axial residual stresses. Axial residual stress is measured using bent-beam test structures [10]. In this method, deformation caused by axial stress is enlarged and transformed into opposite displacements of the verniers (with 0.1 μm resolution) placed at each beam's apex (Fig.2).

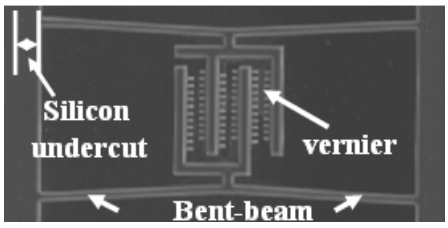


Fig.2. Bent-beam test structure

Table 3 and 4 summarize the measurement results, where the values are from four (Jazz) or six (ST) CMOS-MEMS chips manufactured in the same run. Table 3 and 4 show that structures with field oxide show smaller axial residual stress than structures without field oxide as expected since field oxide is compressive and most beam compositions have tensile axial residual stress.

m4	m3	m2	m1	po	fo	$\bar{\sigma}$ (MPa)
•	•	•	•		•	12.4
•	•	•	•	•	•	15.3
•	•	•	•			21.7
	•	•	•		•	7.2
	•	•	•	•	•	11.9
	•	•	•			18.4
		•	•		•	-0.4
		•	•	•	•	4.4
		•	•			13.2
			•		•	-13.3
			•	•	•	-5.7
			•			-5.8

Table 3. Axial residual stress measurement results from Jazz CMOS-MEMS

m4	m3	m2	m1	po	fo	$\bar{\sigma}$ (MPa)
•	•	•	•		•	-14.8
•	•	•	•	•	•	15.2
•	•	•	•			6.1
	•	•	•		•	57.1
	•	•	•	•	•	58.6
	•	•	•			19.1
		•	•		•	53.9
		•	•	•	•	59.0
		•	•			44.8

Table 4. Axial residual stress measurement results from ST CMOS-MEMS

The error brought on by the 0.1 μm vernier resolution is about 7 MPa. The axial residual stress changes with the silicon undercut shown in Fig. 2. In our measurements, we assume that the silicon undercut is negligible. While at large silicon undercut, the wide section of the bridge (above the silicon undercut area) sustains a negligible part of the axial residual stress and the expression for axial residual stress is different from that in negligible silicon undercut [10]. For

instance, for a Jazz m1-2-3-4 bent-beam with field oxide, a 0.3 μm vernier displacement corresponds to a 13.4 MPa axial residual stress at negligible silicon undercut, while a 9.1 MPa axial residual stress at large silicon undercut. Let us assume that the measurement error of beam width is 10 nm, beam height is 10 nm, effective Young's modulus is 1 GPa, and effective temperature coefficient of expansion is 1 μ/K, the estimated axial residual stress measurement error is about 0.5 MPa.

2.3 Vertical Stress Gradient

Test beams released from the substrate will curl up or down, depending on the relative axial residual stress in the layers. Vertical residual stress is characterized by out-of-plane radius of curvature or, alternatively by vertical stress gradient. The relation between vertical curl (Δz) of test beams (Fig. 3) and out-of-plane radius of curvature (ρ) is

$$\Delta z = 2\rho[\sin(\frac{L}{2\rho})]^2 \quad (2)$$

where L is the beam length. The relation between ρ and vertical stress gradient ($d\sigma_x/dz$) is

$$\frac{d\sigma_x}{dz} = \frac{E}{\rho} \quad (3)$$

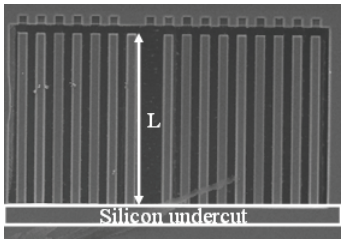


Fig.3. Vertical stress test beams

Table 5 and 6 summarize the measurement results, where the values are from four (Jazz) or six (ST) CMOS-MEMS chips manufactured in the same run. Table 5 and 6 show that structures with field oxide show smaller out-of-plane radii of curvature (i.e., more curl) than structures without field oxide as expected since field oxide is compressive. Large vertical stress gradient is preferable in increasing the self-assembly displacement and the actuation stroke in vertical electro-thermal actuators [11].

Due to silicon undercut shown in Fig. 3, the actual test beam length L', may be longer than the nominal beam length L. We use the nominal beam length L to calculate ρ. A systematical relative error $(L'^2 - L^2)/L^2$ is accompanied with ρ. Since the nominal beam length L is 100 μm, the estimated measurement error brought on by a 10 nm beam length measurement error is negligible.

m4	m3	m2	m1	po	fo	$\overline{\rho}$ (mm)	VSG (Pa/m)
•	•	•	•		•	3.6	$2.00\text{x}10^{13}$
•	•	•	•	•	•	4.1	$1.80\text{x}10^{13}$
•	•	•	•			3.5	$2.09\text{x}10^{13}$
	•	•	•		•	4.1	$1.76\text{x}10^{13}$
	•	•	•	•	•	6.6	$1.12\text{x}10^{13}$
	•	•	•			6.2	$1.18\text{x}10^{13}$
		•	•		•	1.6	$4.56\text{x}10^{13}$
		•	•	•	•	2.0	$2.34\text{x}10^{13}$
		•	•			1.9	$3.89\text{x}10^{13}$
			•		•	0.71	$1.01\text{x}10^{14}$
			•	•	•	0.47	$1.57\text{x}10^{14}$
			•			0.47	$1.70\text{x}10^{14}$

Table 5.Vertical stress gradient (VSG) measurement results from Jazz CMOS-MEMS

m5	m4	m3	m2	m1	po	fo	$\overline{\rho}$ (mm)	VSG (Pa/m)
•	•	•	•	•		•	4.40	$2.09\text{x}10^{13}$
•	•	•	•	•			6.63	$1.42\text{x}10^{13}$
	•	•	•	•		•	2.69	$3.53\text{x}10^{13}$
	•	•	•	•			7.60	$1.29\text{x}10^{13}$
		•	•	•		•	1.82	$5.60\text{x}10^{13}$
		•	•	•			3.08	$3.44\text{x}10^{13}$
			•	•		•	0.77	$1.50\text{x}10^{14}$
			•	•	•	•	1.05	$1.11\text{x}10^{14}$
			•	•			1.45	$8.41\text{x}10^{13}$
			•			•	0.74	$9.80\text{x}10^{12}$
			•				1.23	$6.02\text{x}10^{13}$

Table 6. Vertical stress gradient (VSG) measurement results from ST CMOS-MEMS

2.4 Lateral Stress Gradient

Lateral curl occurs from a stress gradient across the beam width. This lateral stress gradient can arise from layer-to-layer misalignment. The lateral stress gradient can be enhanced by purposefully offsetting the lower metal layers with respect to the top metal layer. This effect is used in self-assembly displacement of lateral electro-thermal actuators [12].

Lateral stress test beams (with the offsetting inner metal width of 1.6 μm, and the top metal width of 2.6 μm) with different compositions manufactured by Jazz and ST processes have been tested. Table 7 summarizes the measurement results from Jazz beams, where the values are from four CMOS-MEMS chips manufactured in the same run. Fig. 4 shows that for some composite ST test beams, the

beam tips displace to the 3 µm limit in the design, which corresponds to an in-plane radius of curvature of less than 1.7 mm and cannot be quantitatively extracted. For instance, ST test structures with four metal conductors (m1-2-3-4) and no polysilicon show an in-plane radius of curvature of 1.4 mm, i.e., a lateral stress gradient of 6.9 x 10^{13} Pa/m. With the same composition, ST structures have smaller in-plane radii of curvature, i.e., larger lateral stress gradient, which is preferable in large actuation stroke applications [12].

The relative error brought on by the vernier resolution (0.1 µm) is $0.1/(\Delta x \pm 0.1)$ where Δx is the lateral curl. Influence of silicon undercut on lateral stress test beam length is negligible. Since the beam length is 100 µm, the estimated measurement error brought on by a 10 nm beam length measurement error is also negligible.

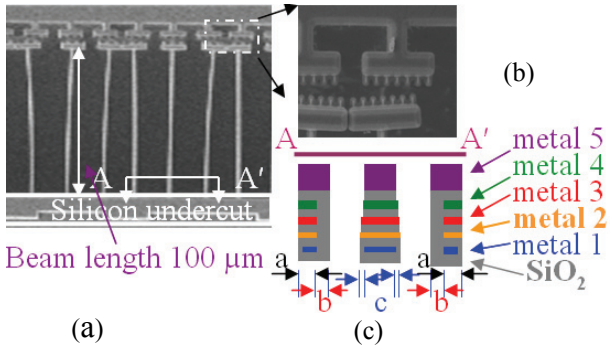


Fig.4. (a) Lateral curls in ST CMOS-MEMS, (b) close-up of the verniers, and (c) cross section and dimensions of some beams. In (c), a = 1.6 µm, b = 1.0 µm, m1 undercut c = 0.3 µm, and m5 are of the same width for these three beams. In the middle beam, the lower metal layer, except m1, is 0.1 µm wider than the adjacent upper metal layer in each side.

m4	m3	m2	m1	po	fo	$\overline{\rho}$ (mm)	LSG (Pa/m)
•	•	•	•		•	19.6	$3.68x10^{12}$
•	•	•	•			18.1	$4.04x10^{12}$
	•	•	•		•	8.2	$8.78x10^{12}$
	•	•	•			5.1	$1.43x10^{13}$
	•		•		•	7.8	$9.23x10^{12}$
	•		•			11.7	$6.24x10^{12}$
		•	•		•	6.4	$1.14x10^{13}$
		•	•			6.1	$1.21x10^{13}$

Table 7. Lateral stress gradient (LSG) measurement results from Jazz CMOS-MEMS

3 DISCUSSION

FEA simulation results verify the experimentally extracted values of effective Young's modulus and axial residual stress, with relative errors less than 1%.

Die-to-die effective Young's modulus variations are 2 GPa for Jazz chips and 3 GPa for ST chips. Measurement errors may be the main reasons for the variations.

Die-to-die axial residual stress variations are 8 MPa for Jazz chips and 20 MPa for ST chips. Vernier resolution and silicon undercut may be the main reasons for the variations.

Die-to-die out-of-plane radii of curvature variations are 1 mm for Jazz chips and 3 mm for ST chips. Silicon undercut may be the main reason for the variations.

Die-to-die in-plane radii of curvature variations are 2 mm. Vernier resolution and misalignment may be the main reasons for the variations.

Naturally balanced narrow beams (all the layers are of the same width and aligned in layout) are not straight after post-CMOS release due to residual stress gradients and process variations. For instance, for a 50 µm long, 0.9 µm wide m1-2 beam, a 0.15 µm lateral curl has been observed after release. The in-plane radius of curvature increases when beam width and/or height increases. To keep the beam straight after post-CMOS release, one can increase beam width or use tapered beam structures by making the lower metal layer wider (0.1 or 0.2 µm in each side) than adjacent upper metal layer [13].

There are several other possible reasons for such wide variations, such as the width variation of each layer, the existence and width variation of the residual plasma which is used in post-CMOS processing, etc. Further characterization of these variations is future work.

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