

Precise 2D Compact Modeling of Nanoscale DG MOSFETs Based on Conformal Mapping Techniques

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ABSTRACT

We present a new technique for 2D compact modeling of short-channel, nanoscale DG MOSFETs. In low-doped devices working in the subthreshold regime, the potential distribution is dominated by the capacitive coupling between the body contacts. This 2D potential is determined by a solution of the Laplace equation for the body using the technique of conformal mapping. Near threshold, where the spatial inversion charge becomes important, a self-consistent solution is applied for the important region around the barrier maximum. In sufficiently strong inversion, the electronic charge will dominate the potential profile in central parts of the channel. For this case, an analytical solution of the 1D Poisson's equation is used. Based on the barrier profiles the drain current was calculated for both drift-diffusion and ballistic transport. The results compare favorably with numerical simulations.

Keywords: MOSFET, double-gate, nanoscale, 2D modeling, conformal mapping.

1 INTRODUCTION

In nanoscale double gate MOSFETs, the dependence on the bias voltages of the 2D electron barrier topology in the conducting channel is all-important for the operation of the device. Here, we discuss the modeling of the device electrostatics, the electron distribution, and the current in various regimes of operation.

In subthreshold, the charge carriers in the low-doped silicon body can be ignored and the electrostatics is dominated by the 2D capacitive coupling between the source, drain and gate electrodes. This allows the potential distribution to be obtained from Laplace's equation for the rectangular DG MOSFET body, using conformal mapping techniques [1]. This precise, analytical 2D solution includes the full dependency of the applied terminal voltages, including any asymmetric biasing of the two gates. Near threshold, where the electronic charge is important, a self-consistent solution is obtained for the potential profile in the vicinity of the energy barrier maximum. In strong inversion, when the electronic charge dominates, an analytical solution of 1D Poisson's equation is adopted.

The solutions for the various regimes of operation are used in the modeling of the drain current based on both drift-diffusion and the ballistic transport mechanisms. Both classical and quantum mechanical approaches have been developed. The modeling results obtained for potential and charge distributions and for the current agree very well with numerical simulations.

The device considered is an *n*-channel device with aluminum gates of length $L=25$ nm, silicon thickness $t_{si}=12$ nm, insulator thickness $t_{ox}=1.6$ nm, and relative dielectric constant $\epsilon_{ox}=7$. The doping density of the *p*-type silicon body is $1 \times 10^{15} \text{ cm}^{-3}$, and that of the *n*-type source/drain contacts are $1 \times 10^{20} \text{ cm}^{-3}$.

2 ELECTROSTATICS

Determining the electrostatics from Laplace's equation for a subthreshold DG MOSFET can be done in different ways, for example, by full Fourier expansion of the potential or by using a low-order truncation [2-4]. The alternative approach considered here is to apply the conformal mapping technique, which was first used for classical, long-channel MOSFETs [5]. Later, the technique was enhanced and applied to sub-100 nm bulk MOSFETs [6] and to the subthreshold and nearthreshold regimes of low-doped DG MOSFETs [7-9]. Here, we present modeling details and include new modeling results for a wider range of device operation.

2.1 Subthreshold

To describe the device electrostatics, we replace the insulator by an electrostatically equivalent silicon layer with thickness of $t'_{ox}=t_{ox}\epsilon_s/\epsilon_{ox}$, where ϵ_s is the relative permittivity of silicon. We then consider Laplace's equation for this extended body whose boundary is defined by the inner surfaces of the gate contacts, the source, the drain, and the gaps between the contacts in the four corners. In the strongly doped source/drain contacts, the depletion widths will be small compared to the body dimensions and can initially be neglected.

The boundary condition of Laplace's equation is defined by the potentials of the four contacts, each of which is assumed to be equipotential, and the effective potential drops across the four insulator gaps between them. All

potentials are referenced to that of a fictitious neutral point of the silicon body. Hence, the source contact is at the built-in voltage V_{bi} and the drain contact is at the potentials $V_{bi}+V_{DS}$, assuming a drain-source bias of V_{DS} . The surface potential at the gate electrodes is $V_{GSi}-V_{FB}$, where V_{GSi} is the applied bias between gate i (1 or 2) and source, and V_{FB} is the flat-band voltage between the gate and the body. The 2D potential distribution $\phi(x,y)$ (and electrical fields) in the device body is indicated schematically in the device cross-section of Fig. 1a. The body, described in the normal (x,y) -plane, is mapped into the upper half of the complex (u,iv) -plane, where the boundary of the extended body is mapped into the real u -axis [7], as shown in Fig. 1b.

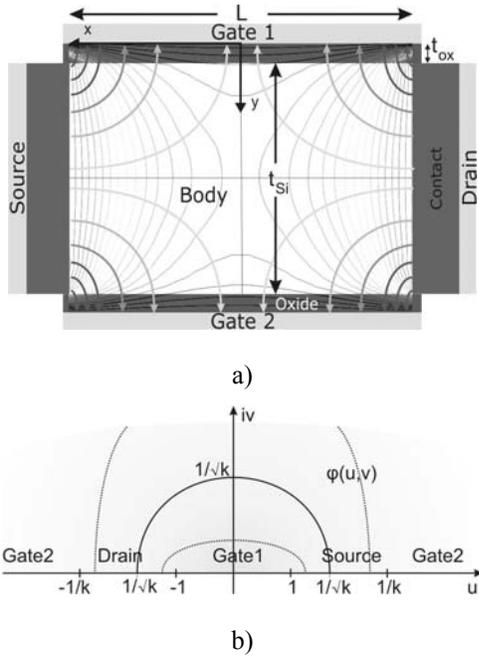


Figure 1: Schematic view of the DG SOI MOSFET device structure (a). In the mapped extended body (b), the u -axis, the iv -axis and the circle of radius $1/\sqrt{k}$ represent the boundary, the central gate-to-gate and source-to-drain symmetry lines, respectively. The ellipse-like shapes represent other lines parallel to the gates in a).

For the rectangular body, the mapping is defined by the following Schwartz-Christoffel transformation:

$$z = x + iy = \frac{L}{2} \frac{F(k, w)}{K(k)} \quad (1)$$

where

$$F(k, w) = \int_0^w \frac{dw'}{\sqrt{(1-w'^2)(1-k^2w'^2)}} \quad (2)$$

Here, $F(k, w)$ with $w=u+iv$ is the elliptic integral and $K(k) \equiv F(k, 1)$ is the complete elliptic integral, both of the first kind. The modulus k is a constant between 0 and 1 determined by the geometric ratio $L/(t_{Si}+2t'_{ox})$. Real arguments $w=u$ define the boundary of the extended body and $u=0$, corresponding

to $x=0$, defines the middle point on the upper gate contact (Gate 1). The four corners of the body map to $u=\pm 1$ and $u=\pm 1/k$. The middle point in the lower gate contact (Gate 2) is at $u=\pm\infty$ and $v=\infty$.

In the standard range $0 \leq u \leq 1$, many approximate expressions, series expansions, and iteration routines exist for $F(k, u)$. $F(k, w)$ can also be expressed in terms of the standard elliptic integral along the entire boundary and along the two symmetry axes [9]. In addition, routines exist for calculating the values for general complex arguments. Further details on the mapping can be found in [7-9].

The potential distribution throughout the extended body can generally be expressed in the (u, iv) -plane as [1]

$$\phi(u, v) = \frac{v}{\pi} \int_{-\infty}^{\infty} \frac{\phi(u')}{(u-u')^2 + v^2} du' \quad (3)$$

where $\phi(u')$ is the electrostatic potential along the boundary. Eq. (3) results in the following analytical expression for the potential distribution in the w -plane [8]:

$$\phi(u, v) = \frac{1}{\pi} \left\{ \begin{aligned} & \left[(V_{GS2} - V_{FB}) \left[\pi - \tan^{-1}\left(\frac{1-ku}{kv}\right) - \tan^{-1}\left(\frac{1+ku}{kv}\right) \right] \right. \\ & + (V_{GS1} - V_{FB}) \left[\tan^{-1}\left(\frac{1-u}{v}\right) + \tan^{-1}\left(\frac{1+u}{v}\right) \right] \\ & + V_{bi} \left[\tan^{-1}\left(\frac{1-ku}{kv}\right) - \tan^{-1}\left(\frac{1-u}{v}\right) \right] \\ & \left. + (V_{bi} + V_{DS}) \left[\tan^{-1}\left(\frac{1+ku}{kv}\right) - \tan^{-1}\left(\frac{1+u}{v}\right) \right] \right] \end{aligned} \right\} \quad (4)$$

Here, only the major terms associated with the inner equipotential contact surfaces are considered. Equation (4) is the exact solution in the limit of zero insulator thickness. In our calculations, correction terms associated with the corner insulator gaps are added to improve the accuracy of $\phi(u, v)$. This distribution can now be mapped to the real (x, y) -plane using the transformation of Eq. (1).

Figure 2 shows the 2D potential distribution for our device, calculated from Eq. (4) using $V_{DS}=0.5$ V and $V_{GS1}=V_{GS2}=-0.45$ V [9]. At $V_{DS}=0$ V, $\phi(x, y)$ has a saddle point at the device center, corresponding to the minimum barrier energy for electron conduction between source and drain. With increasing V_{DS} , the barrier minimum is steadily lowered and shifted towards the source. This drain-induced barrier lowering (DIBL) is intrinsic to the present formalism as expressed in Eq. (4). An excellent agreement between the present model and numerical calculations using the Atlas device simulator has been demonstrated [8]. With increasing, symmetric gate biasing, the gate-to-gate barrier energy profile is lowered and flattens, and the barrier minimum eventually shifts to the silicon-insulator interfaces near threshold. At this stage, the induced electron density will strongly influence the device electrostatics, requiring a self-consistent analysis (see Section 2.2).

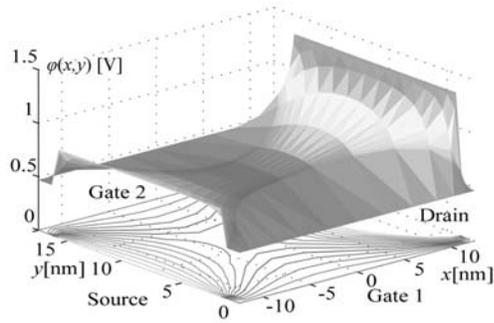


Figure 2: Potential distribution over the extended body at subthreshold condition ($V_D=0.5$ V and $V_{GS1}=V_{GS2}=-0.45$ V) calculated from Eq. (4) and mapped to the (x,y) -plane using the mapping function in (1).

The quasi-equilibrium 2D electron density distribution in subthreshold can be calculated from the potential distribution $\phi(x,y)$ using either a Boltzmann type classical expression or a formalism based on energy level quantization perpendicular to the gates. In the latter case, we assume a deep energy well with steep walls, where the topography of the bottom of the well is contained in $\phi(x,y)$. Considering the case of $V_{DS}=0$ V, the subband energy levels and wave functions can be calculated for the central gate-to-gate symmetry axis. For the present device, the potential variation along this axis is very close to parabolic, such that we can use harmonic oscillator solutions for the lowest energy levels within the parabola and perturbed square-well solutions for higher energy levels.

Figure 3 shows a comparison of modeled and simulated electron density distributions along the central gate-to-gate symmetry line for $V_{GS}=-0.47$ V. The results are based on the classical formalism (model and Atlas) and on the quantum mechanical approach (model). We observe good agreement between the model calculations and the Atlas simulation, and between the classical and quantum mechanical approach.

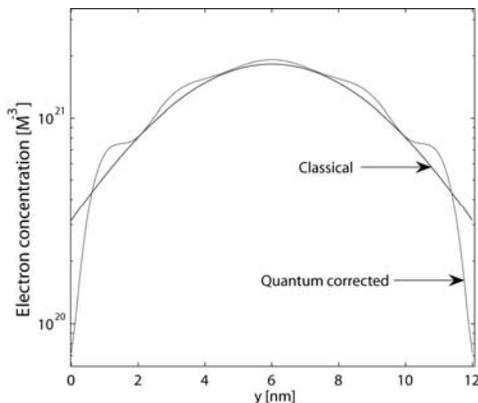


Figure 3: Comparison of modeled and simulated electron density distributions along the gate-to-gate symmetry line at $V_{GS}=-0.47$ V [7].

The device threshold voltage V_T can be defined in several ways, for example, in terms of a minimum current level, a minimum electron sheet density, or, as is usually done for the classical MOSFET, as the gate bias that causes a band bending by twice the silicon body Fermi potential at the barrier minimum. Using the latter definition, we find from the potential distribution of Eq. (4) that $V_T=-0.47$ V for symmetric gates and zero drain bias [8]. For the other definitions, V_T will be higher, around -0.1 V.

An important signature of short-channel effects is the DIBL effect (see above). From Eq. (4), we can model V_T versus drain voltage as shown in Fig. 4 for both symmetric and asymmetric gate bias.

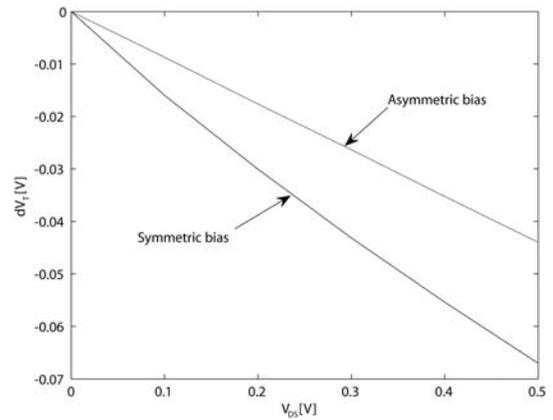


Figure 4: Comparison of drain-induced barrier lowering dV_T for symmetric and asymmetric gate bias [8].

2.2 Near threshold

Near and above threshold, the carrier contribution to the body potential cannot be neglected. In this case, Poisson's equation is divided into two superimposed parts, the first of which is the 2D capacitive coupling (see Section 2.1). The second part accounts for how field lines emanating from charge carriers are distributed over the four electrodes. A simplified estimate considers only the associated perpendicular electric field on the gate electrodes near the maximum of the channel barrier, which is the part that has the greatest influence on the drain current. In subthreshold and moderately strong inversion, an overall parabolic shape of the gate-to-gate potential profile can be assumed at this location, which is in excellent agreement with numerical simulations performed for the device considered. Using this approximation, a self-consistent solution can be obtained by determining the height of the parabola (ϕ_m) by means of a simple iterative routine.

Assuming a classical electron distribution, we consider specifically the gate-to-gate energy barrier at the middle of the device for $V_{GS1}=V_{GS2}$ and $V_{DS}=0$ V. Since the DIBL-effect is embedded in Eq. (4), it carries over to the calculation of the modified, self-consistent gate-to-gate barrier profile. For the drain current modeling (see Section

3), we have adopted a simplified approach where we assume that the total gate-to-gate potential distribution $\varphi(y)$ for finite values of V_{DS} retains the same, near-parabolic form as for $V_{DS}=0$ V, but scaled to reflect the correct barrier minimum as dictated by the DIBL-effect.

Along the gate-to gate symmetry line, we superimpose the 1D potential contribution $\varphi_1(y)$ from the free electrons and the 2D contribution $\varphi_2(y)$ from the capacitive coupling to obtain $\varphi(y)=\varphi_1(y)+\varphi_2(y)$.

Classically, $\varphi_1(y)$ is determined by integrating twice the 1D Poisson equation for $\varphi(y)$ using Boltzmann statistics for the electron density inside the silicon layer. This leads to a self-consistent expression for $\varphi_1(y)$ in the form of an integral equation. To solve this, we approximate $\varphi(y)$ by a symmetric parabolic form with a maximum deviation φ_m from its boundary value $V_{GS}-V_{FB}$. For thin devices as here, this approximation is found to agree very well with numerical simulations within the operating range considered. By adding the resulting, explicit expression for $\varphi_1(y)$ to $\varphi_2(y)$ from Eq. (4), we obtain the following implicit, algebraic equation from which the parameter φ_m can easily be extracted [9],

$$\begin{aligned} \varphi_m = & \left[\frac{4}{\pi} \tan^{-1} \left(\frac{1}{\sqrt{k}} \right) - 1 \right] (V_{bi} - V_{GS} + V_{FB}) \\ & - \frac{qn_i^2 (t_{Si} + 2t'_{ox})^2}{8\epsilon_s N_a} \exp \left(\frac{V_{GS} - V_{FB} + \varphi_m}{V_{th}} \right) \\ & \times \left\{ \text{sgn}(\varphi_m) \sqrt{\frac{\pi V_{th}}{\varphi_m}} \text{erf} \left(\sqrt{\frac{\varphi_m}{V_{th}} \left(1 - \frac{2t'_{ox}}{t_{Si} + 2t'_{ox}} \right)} \right) \right. \\ & \left. + \frac{V_{th}}{\varphi_m} \left[\exp \left(-\frac{\varphi_m}{V_{th}} \left(1 - \frac{2t'_{ox}}{t_{Si} + 2t'_{ox}} \right)^2 \right) - 1 \right] \right\} \end{aligned} \quad (5)$$

where N_a is the body doping density, V_{th} is the thermal voltage, erf is the error function, and sgn returns the sign of the argument φ_m . Figure 5 shows a comparison of the potential φ_m versus applied V_{GS} for $V_{DS} = 0$ V as calculated from Eq. (5) and simulated classically in Atlas.

Note that in the model calculations, we have adjusted V_{bi} to include the effects of a finite depletion width inside the source and drain. We observe an excellent agreement between the model and the simulation within the range of V_{GS} considered.

A more rigorous approach is to calculate the self-consistent barrier profile quantum mechanically. As an example of such an analysis, we consider the special case of a flat potential well where $\varphi(y)=V_{GS}+V_{FB}$. This situation takes place very near threshold when the barrier topology changes from the shape of a saddle point to that of an extremal point as a result of the combined and compensating actions of capacitive coupling and induced electronic charge. Therefore, since $\varphi_2(y)$ is close to parabolic (see above), a flat quantum well requires that $\varphi_1(y)=\varphi_2(y)-(V_{GS}+V_{FB})$, i.e., the two quadratic contributions must cancel. Moreover, a parabolic $\varphi_1(y)$ is obtained for a flat electron density $n(y)$ at the barrier (except near the

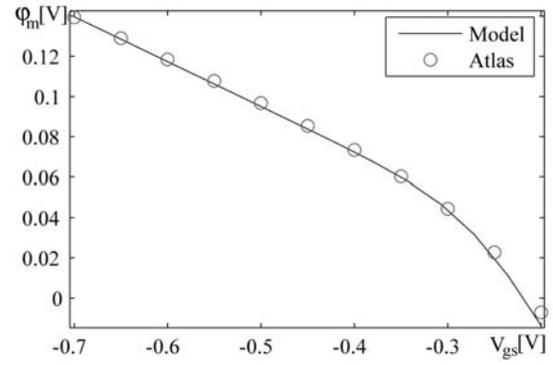


Figure 5: Comparison of φ_m versus V_{GS} for $V_{DS}=0$ V between calculations based the present model (Eqs. (5) and solid curves and numerical simulations performed with Atlas (circles).

silicon-insulator interface where quantum mechanics requires that $n(y)$ drops to zero).

Hence, using the standard expression for the electronic subband energies and wave functions for a 2D electron gas in a flat potential well, we can write the following expression for the flat electron sheet density for each of the two gate electrodes (derived for the device center):

$$n_s = \frac{k_B T}{6\pi\hbar^2} \sum_{\text{valleys}} \sum_j m_i \ln \left[1 + \exp \left(-\frac{E_g/2 + E_{ij} - q(V_{GS} - V_{FB} - \varphi_b)}{k_B T} \right) \right] \quad (6)$$

where E_g is the band gap energy of the silicon body, φ_b is the Fermi potential of the doped silicon body referred to that of intrinsic silicon, the index j runs over the the subbands of a given conduction band valley, and i runs over the six valleys with subband masses m_i and minimum subband energies E_{ij} . This leads to an implicit, self-consistent expression for the V_{GS} which corresponds to the flat-band condition. This value agrees well with the result obtained for the classical case by setting $\varphi_m=0$ V in Eq. (5).

2.3 Strong inversion

Well above threshold, the carriers tend to screen out the influence of the drain and source electrodes, allowing us to treat the capacitive coupling in the device interior as a perturbation. At sufficiently high electron concentrations, the barrier develops a flat section dominated by the charge carriers. In this case, the potential profile can be calculated according to the long-channel solution [10,11]. Moreover, adjusting for the effects of the Fermi potential of the doped body, the threshold voltage can be expressed as $V_T=V_0+2\varphi_b$, where V_0 is given by the following implicit expression valid for $V_{GS}>V_0$

$$V_0 = \phi_{ms} + \frac{2k_B T}{q} \ln \left(\frac{\epsilon_{ox} t_{Si} (V_{GS} - V_0)}{2t_{ox} q n_i} \right) \quad (7)$$

Here, ϕ_{ms} is the work function difference between the gate metal and intrinsic silicon. We note that well-defined channels develop along the silicon-insulator interfaces in strong inversion, where the flat section defines an effective channel length, which is close to the physical gate length, as indicated in the simulated (Atlas) potential contour plot shown in Fig. 6. This allows the drain current to be described with a traditional long-channel expression, see Section 3.1.

Quantum mechanically, the strong inversion channels can be considered to be near-triangular, allowing the electron energy quantization to be described in terms of an Airy-function model. Above the top of the barrier, the quantization can be done by perturbed flat-well solutions.

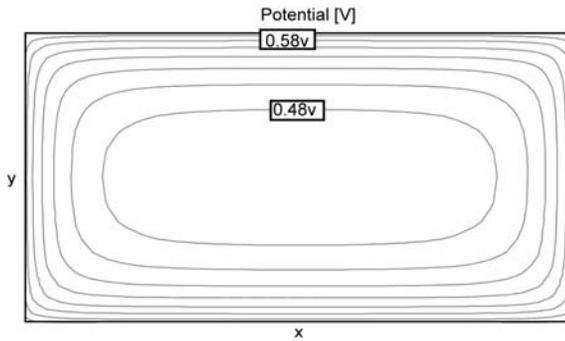


Figure 6: Contour plot of the present DG MOSFET simulated with Atlas for $V_{DS}=0$ V and $V_{GS}=0.1$ V, indicating well-established conducting channels near gates.

3 DRAIN CURRENT

In nanoscale MOSFETs, with channel lengths less than about 50 nm, the relaxation times of the carriers indicate that the drain current will have the character of both drift-diffusion and ballistic/quasi-ballistic transport. Therefore, we consider drain current models based on both of these mechanisms.

3.1 Drift-diffusion transport

In subthreshold and near threshold, the current is relatively small and its influence on the barrier topology can be ignored. This allows us to use the following simple and explicit drift-diffusion model for the current that relies on the shape of the barrier near its maximum [12],

$$I_{DD} = 2qW\mu_n V_{th} \left(1 - e^{-V_{DS}/V_{th}}\right) \int_0^L \frac{dx}{n_{so}(x)} \quad (8)$$

Here, W is the device width, μ_n is the electron mobility, $V_F(x)$ is the quasi-Fermi potential in the channel, and $n_{so}(x)$ is the sheet electron density in each of the two channels, obtained from the analysis of the electrostatics in Sections

2.1 and 2.2. Note that in Eq. (8), we implicitly assume a constant quasi-Fermi level $V_F(x)$ from source through the barrier.

As indicated in Section 2.3, the strong inversion drain current can be modeled below saturation as follows (simple charge control model) [11],

$$I_{DD} = \frac{2W\mu_n t_{ox}}{\epsilon_{ox} L} \left(V_{GT} V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (9)$$

Here $V_{GT}=V_{GS}-V_T$, where the threshold voltage V_T is defined in Section 2.3. Note that more elaborate, traditional 1D current models, including saturation, can be used as well. Also, the quantum mechanical exclusion of electrons near the gate insulator has not been included in Eq. (9).

Figure 7 shows a comparison between the modeled drift-diffusion transfer characteristics obtained from Eqs. (8) (subthreshold and near threshold) and (9) (strong inversion) and the corresponding characteristics obtained from the Atlas device simulator. The ranges of the model calculations are shown as solid curves. These are connected by dashed sections in the range where the present models are invalid. Also, for a true comparison with the simulated curves, the parasitic resistances associated with the simulated device have been extracted and included in the modeled curves. We observe a very good agreement between modeled and simulated results within the ranges of V_{GS} considered.

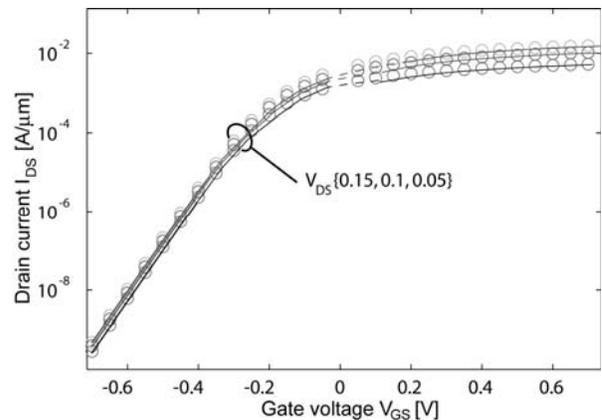


Figure 7: Drift-diffusion transfer characteristics. Comparison between model calculations (solid curves) and Atlas simulations (circles). Dashed sections in the midrange of the curves are extrapolated tendencies.

3.2 Ballistic transport

Ballistic transport means that the charge carriers (electrons) are injected into the channel from source and drain, and that those with suitable energies traverse the channel without scattering [13, 14]. In this case, the current will be limited by the injection process. To some degree,

backscattering, which gives rise to so-called quasi-ballistic transport can be taken into account by means of a reflection coefficient [15]. Here, only ballistic transport is considered.

Using a formalism first investigated by Natori [13], we can write the ballistic current as $I_{BT}=q(F^+-F^-)$ where F^+ and F^- are the carrier fluxes emitted from the source and the drain, respectively, given by:

$$F^\pm = \frac{(2k_B T)^{3/2}}{\pi^2 \hbar^2} \sum_{\text{valleys}} \sum_j \sqrt{m_i} F_{1/2} \left(\frac{E_{F_s} - E_{ij} - qV^\pm}{k_B T} \right) \quad (10)$$

$F_{1/2}$ is here the 2D Fermi function of order $1/2$, E_{F_s} is the Fermi level at the source, $V^+ = 0$ V (source) and $V^- = V_{DS}$ (drain). Note that E_{ij} are the quantum levels associated with the channel barrier, which can be derived from the analysis of the electrostatics in Section 2. In this case, they are not much influenced by the drain current.

Figure 8 shows a comparison between the modeled ballistic transfer characteristics from deep subthreshold to strong inversion, and the corresponding characteristics obtained from the Atlas device simulator using a hydrodynamic model. Here, we used the approximations to Eq. (10) discussed in Ref. [14]. Again, the ranges of the model calculations are shown as solid curves, connected by extrapolations (dashed sections).

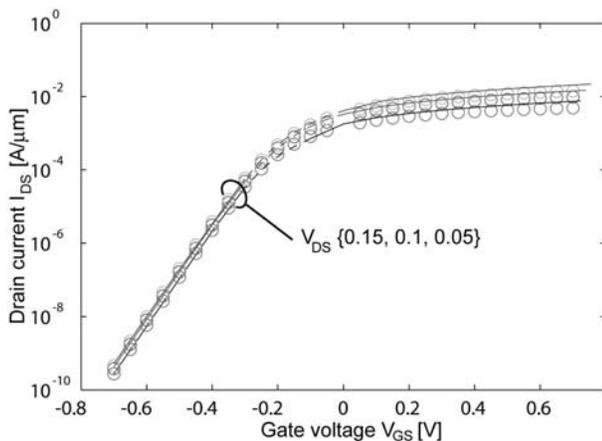


Figure 8: Modeled ballistic transfer characteristics (curves) compared with Atlas simulations using a hydrodynamic model (circles). Dashed sections in the midrange of the curves are extrapolated tendencies.

Again, we observe an overall good agreement between the modeled and simulated results. However, as expected, the model gives a somewhat higher current in strong inversion owing to the omission of scattering. A point of interest is that the drift-diffusion and the ballistic transport mechanisms have a good mutual agreement in the characteristics, both for the model and for the simulations.

4 CONCLUSION

We have developed a precise, compact 2D model for the capacitive coupling between the electrodes in lightly doped

nanoscale DG MOSFETs based on the technique of conformal mapping. Combined with the electrostatic effects of the inversion charge carriers, we have been able to incorporate the 2D effects in a self-consistent analysis of the channel barrier topography in the subthreshold and near threshold regimes of operation. Short-channel effects, including DIBL, are inherently contained in this analysis, and no adjustable parameters are used. In strong inversion, where the effects of the electron charge dominate, the problem reduces to that of a long-channel device. Associated drain current models have been described for both drift-diffusion and ballistic transport. The modeled device electrostatics and drain currents agree very well with numerical simulations using the Atlas device simulator from Silvaco.

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