Instability in flatband voltage of SiO_2 embedded with silicon nanocrystals

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ABSTRACT

In this work, the flatband voltage shift of SiO_2 embedded with silicon nanocrystal (nc-Si) annealed at different annealing temperature, different annealing time and under different temperature ramping rates are being investigated. The Si-ions are implanted into the SiO_2 with very low energy. The instability of the flatband voltage shift is due to fact that there are remaining Si ions in the SiO_2. It is observed that the flatband voltage shift can be reduced to a minimum of -0.1 V when the sample is annealed at 900 ^oC for 20 mins using the conventional furnace annealing process. In contrast, rapid thermal annealing at 900 ^oC for 100 s is not possible to eliminate the remaining Si ions. The number of remaining Si ions is found to be ~ 0.2 % of the total implanted doses.

Keywords: silicon nanocrystal, flatband voltage, silicon dioxide

1 INTRODUCTION

Silicon nanocrystal (nc-Si) embedded in SiO_2 thin film can be produced by several methods, including ion-implantation, chemical vapor deposition, sputtering, pulse laser deposition and others. Recently, low-energy ion implantation has been used to produce nanocrystal embedded in the dielectric film for the application of nonvolatile memory devices [1-3]. This technique is fully compatible with the mainstream CMOS process and the distribution of nc-Si in the gate oxide can be easily controlled. To produce the nc-Si in the dielectric film, the Si-ions are implanted into the thin film, and subsequently thermal annealing in N_2 ambient is carried out at high temperature [4]. Too much thermal budget will cause problems for the devices. Besides, there is a question concerning the Si ions trapped in the SiO_2 matrix. Although the Si ions can be removed by a high temperature annealing, there may be some Si-ions still remaining if the annealing temperature is not high enough or the annealing time is not long enough. Insufficient thermal budget will lead to the existence of residual Si-ions in the SiO_2 matrix, which will definitely affect the flatband voltage of the memory devices. Currently there is a lack of study on the impact of annealing temperature and duration on the device's flatband voltage shift. In this work, we have studied the flatband voltage instability under the condition of different annealing temperature and annealing time. Moreover, the influence of different temperature ramping rates on the flatband voltage shift is also being investigated. On the other hand, the number of excess Si trapped inside the SiO_2 after annealing is also being investigated.

2 EXPERIMENTAL

30 nm SiO_2 thin film was thermally grown in dry oxygen at 950 ^oC on a boron doped p-type Si(100) wafer. Si^+ with a dose of 8×10^{16} cm^{-2} were then implanted into the SiO_2 thin films at the energy of 1.3 keV. Thermal annealing was carried out in N_2 ambient at various annealing temperatures for different annealing time. It has a temperature ramping rate of ~10 ^oC/min and it is known as conventional furnace annealing. Another 30 nm SiO_2 was implanted with 1×10^{16} cm^{-2} Si ions at the energy of 2 keV. The annealing is carried out at different temperatures with the temperature ramping rate of ~40 ^oC/s. This type of annealing is known as rapid thermal annealing. As-implanted (no annealing) samples are also included in this study. Platinum thin films were deposited and patterned to form the top and bottom electrodes. Capacitance-voltage (C-V) measurements were performed at the frequency of 1 MHz with a HP4284A LCR meter at room temperature.

3 RESULTS AND DISCUSSIONS

Fig. 1 shows the flatband voltage shift as a function of both the annealing temperature and annealing time for the conventional furnace annealing. The annealing experiments were carried out with either a constant annealing time or a constant annealing temperature. For the former case, the annealing time is set at 20 mins and the annealing temperature varies from 500 ^oC to 1100 ^oC. For the latter case, the annealing temperature is set at 1000 ^oC and the annealing time varies from 20 mins to 100 mins. The flatband voltage shift (ΔV_{fb}) is measured with respect to the flatband voltage of a 30 nm pure SiO_2 sample. In this figure, it is observed that the as-implanted sample also experience some annealing effect during the deposition of platinum electrodes.

The as-implanted sample has the largest negative flatband voltage shift (~ -38 V), while the flatband voltage shift gradually reduces as the annealing temperature increases as shown in Figure 1. The flatband voltage shift is -35 V, -28 V and -10 V for the sample annealed at 500 ^oC,

600 °C and 700 °C, respectively. At annealing temperatures > 900 °C, no further reduction in the flatband voltage shift is observed, and the ΔV_{fb} is ~ -0.1 V. This shows that the annealing temperature has reached a saturation point and no further reduction in the flatband voltage shift can be obtained even if the annealing temperature is increased to 1100 °C.

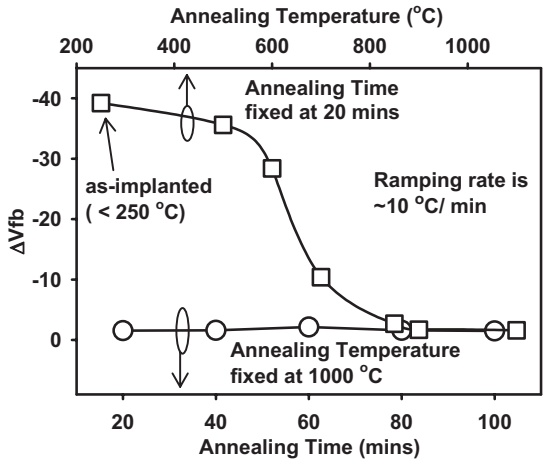

Figure 1: Flatband voltage shift as a function of both annealing temperature and annealing time for conventional furnace annealing.

For the case of annealing temperature fixed at 1000 °C, the annealing time varies from 20 mins to 100 mins. An almost constant ΔV_{fb} ranging from -0.2 V to -0.1 V is observed for annealing time longer than 20 mins, as shown in Figure 1. This clearly indicates that the annealing carried out at 900 °C for 20 mins is good enough as a higher annealing temperature or a longer annealing time does not reduce the flatband voltage shift further. This has an important implication for memory device fabrication when the thermal budget constrain is important.

We further investigated the flatband voltage shift of implanted Si-ions in the SiO_2 thin film annealed under the rapid thermal annealing (RTA) process. RTA process has been used frequently in CMOS process especially on the dopant activation [5]. Fig. 2 shows the flatband voltage shift as a function of different annealing temperature and annealing time using the rapid thermal annealing (i.e., ramping rate = ~40 °C/ s). For the as-implanted sample, the flatband voltage shift is still very large (~ -37 V). There is a gradual reduction of flatband voltage shift as the annealing time increases from 20 s to 100 s for the sample annealed at 900 °C. There is still a large flatband voltage shift (~ -22 V) even though the sample has been annealed at 900 °C for 100 s using the RTA process. Besides, it is found that the flatband voltage shift is still very high even though the sample is being annealed at 1000 °C for 20 s. The flatband voltage shift is ~ -13 V. Comparing to the samples annealed using the conventional furnace annealing at 900 °C for 20 mins, the flatband voltage shift has been reduced to a minimum value. As such, RTA process is still not possible to remove the remaining Si ions inside the SiO_2.

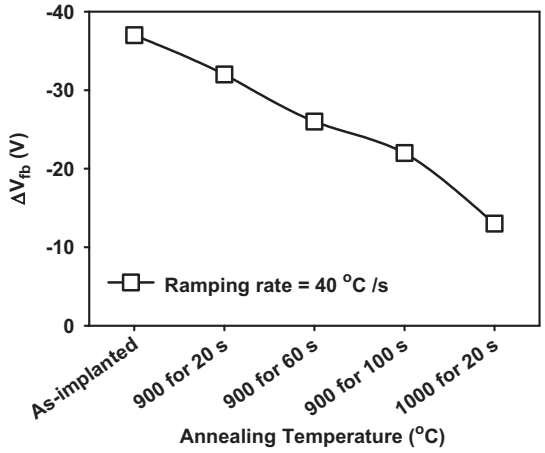

Figure 2: Flatband voltage shift for the sample annealed by rapid thermal annealing (RTA) process.

The number of trapped Si ions can be determined from the flatband voltage shift. We assume that the distribution of the charge density ρ(x) due to the trapped Si ions in the SiO_2 thin film is proportional to the distribution of the implanted Si in the SiO_2 thin film, i.e., ρ(x) = A*f(x)* where A is a coefficient depending on thermal annealing and *f(x)* is the distribution of the implanted Si. The distribution of the implanted Si can be determined from the stopping and range of ions in matter (SRIM) simulation or from the Secondary Ion Mass Spectroscopy (SIMS) measurements. The number of remaining Si ions, *N* is found to be

$$N = \frac{(C_{ox}\Delta V_{fb})}{1.6\times10^{-19}} \frac{T_{ox}\int_0^{T_{ox}} f(x)dx}{\int_0^{T_{ox}} xf(x)dx} \qquad (1)$$

where T_{ox} is the SiO_2 thickness, and C_{ox} (= $\frac{\varepsilon_r\varepsilon_0}{T_{ox}}$ where ε_r is the dielectric constant of SiO_2 and ε_0 is the permittivity in vacuum) is the gate oxide capacitance per unite area.

Fig. 3 shows the number of trapped Si ions as a function of different annealing temperature and annealing time. These samples are annealing using the conventional furnace annealing process. The as-implanted sample has ~ 1.5×10^{14} ions/cm^2 of Si-ions trapped in the SiO_2. This means that only ~ 0.2 % of the implanted ions (note that the implant dose is 8×10^{16} ions/cm^2) remains in the SiO_2 thin film for

the as-implanted sample. For the sample annealed at 900 °C for 20 minutes, thermal annealing has reduced the number of the trapped ions to the lowest limit (i.e., ~1×10^{12} ions/cm^2). At higher annealing temperature (i.e., 1000 °C or 1100 °C for 20 mins), there is no further reduction in the number of trapped Si ions. When the annealing time (at 1000 °C) is increased, there is also no further reduction in the number of trapped Si ions.

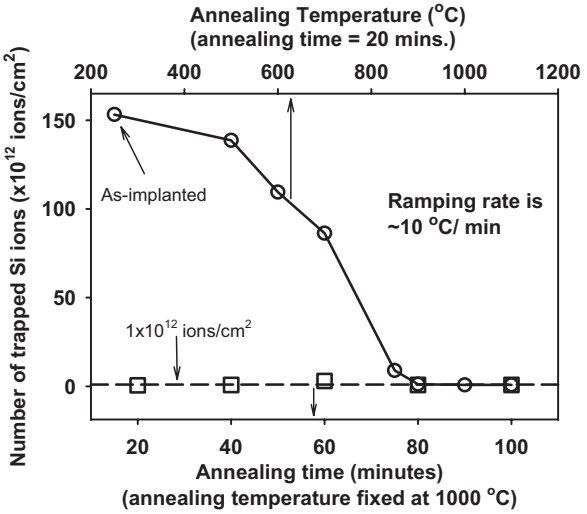

Figure 3: Number of trapped Si ions as a function of both annealing temperature and annealing time for conventional furnace annealing.

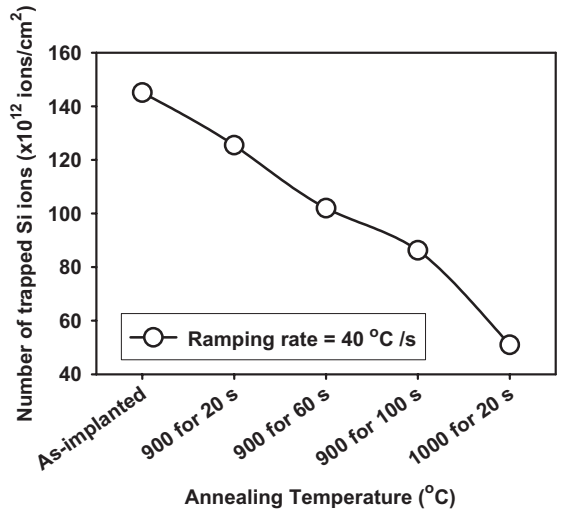

Figure 4: Number of trapped Si ions as a function of both annealing temperature and annealing time for rapid thermal annealing.

Fig. 4 shows the remaining trapped Si ions in the SiO_2 when the sample is annealed with RTA process. For the sample annealed at 1000 °C for 20 s, the remaining Si ions is found to be ~5.1×10^{13} ions/cm^2, which is 50 times larger than that of the sample annealed using the conventional furnace annealing. Similarly to the sample annealed at 900 °C, the remaining trapped Si-ions is about 86 to 125 times larger when the annealing time reduces from 100 s to 20 s. This indicates that it is difficult to eliminate the Si ions by using the RTA process.

4 CONCLUSION

The flatband voltage shift of SiO_2 embedded with silicon nanocrystal (nc-Si) annealed at different annealing temperature, different annealing time and under different temperature ramping rates has been investigated. The effect of Si ions trapped in the gate oxide on the C-V characteristics and the flatband voltage has been examined through the thermal annealing experiments. The flatband voltage shift due to the trapped Si ions can be reduced drastically by conventional furnace annealing. At the annealing temperature of 900 °C and the annealing time of 20 mins, the Si ions trapped in the SiO_2 can be reduced to a minimum value of ~0.2 % of the total implanted Si ions and the flatband voltage shift is ~ -0.1 V.

5 ACKNOWLEDGEMENT

This work has been financially supported by the Ministry of Education Singapore under project No. ARC 1/04 and also supported by the Singapore Millennium Foundation (SMF).

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