

SPICE Modeling of Multiple Correlated Electrical Effects of Dopant Fluctuation

Y.M. Lee*, J.S. Watts, S. Grundon, D. Cook and J. Howard
IBM Semiconductor Research and Development Center
1000 River Road, MS/972F, Essex Junction, Vermont USA
Tel: (802)769-8882, Fax: (802)871-7761, Email: *yoomi@us.ibm.com

ABSTRACT

We proposed a new methodology capable of accurately modeling the partial correlations and geometric dependence in the local random fluctuations of various electrical parameters. This method incorporates principal factor analysis (PFA) into the conventional SPICE-based compact modeling of the mismatch variation which is only focused on the dependence of the variation on device's geometry and biases. PFA enables one to model correlations among the fluctuations by determining the dominant factors and their weights contributed to each of electrical parameter variations. This new methodology enables a better prediction in both digital and analog circuit performance spread because the Monte Carlo model will cover the comprehensive range of transistor variation without creating unrealistic cases.

Keywords: random dopant fluctuation, compact modeling, principal factor analysis, threshold voltage mismatch

1 INTRODUCTION

The random local fluctuations, so called mismatch variation, of the threshold voltage (V_T) and channel current (I_{DS}) in MOSFETs is becoming one of the bottlenecks in process scaling for the advanced CMOS technologies. As transistors shrink and VDD is downscaled, mismatch variations mainly caused by dopant fluctuations are becoming a significant contribution toward the total variation of individual FETs in many applications. As a result, designers have less design margin available and therefore require more accurate models for this physical phenomena.

Traditionally SPICE-base compact modeling work has focused only on predicting the magnitude and geometric dependence of mismatch variations in V_T and I_{DS} between matched FETs, not on correlation in them [1]-[2]. Due to the physical causes of the fluctuation, there exist correlations in local fluctuations [3] of various electrical parameters. Since BSIM model does not explain the effects of number of dopant or its position in the channel region on electrical parameters, it is difficult to cover the correlation found in various electrical parameters using only the BSIM model.

The new methodology introduced here is capable of modeling the correlation without sacrificing accuracy of the dependence on device sizes. Incorporating principal factor analysis (PFA) into SPICE-base compact modeling

provides 1) vectors for the dominant independent components and 2) partial correlations for electrical parameter variation contributed to each of dominant components.

2 MODELING FLOW

The conceptual modeling diagram in two dimensional spaces is shown Figure 1. The ellipsoid in the diagram is a distribution of the mismatch variation of the electrical parameter E_1 and E_2 . The independent random unit distributions, P_1 and P_2 identified by PFA, are propagated to the SPICE model parameter distributions, M_1 and M_2 , which reproduce in simulation the mismatch distribution of electrical parameters, E_1 and E_2 . The modeling goal here is to find mathematical relationships for the SPICE model parameter distributions, M_1 and M_2 , in terms of independent random unit distributions, P_1 and P_2 .

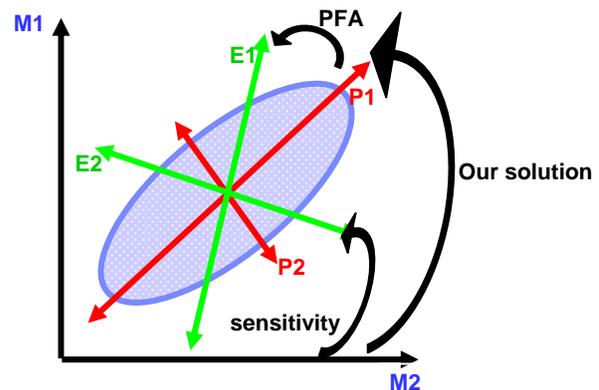


Figure 1: Matrix rotation from BSIM model parameter spaces to electrical parameter spaces via principal component spaces.

In order to implement the ellipsoid distribution into the SPICE model, there are 3 main steps involved for each device size; 1) performing principal factor analysis on electrical parameters, 2) obtaining sensitivity matrix of model parameters to electrical parameters, and 3) solving the mismatch correlation coefficient matrix. Then the information for all geometries is combined in a single model by linear regression. The detail illustrations are followed.

As a first step, PFA is performed on electrical parameters. PFA generates a matrix which rotates P_1 and P_2 space to E_1 and E_2 space. The matrix expression is,

$$[E] = [L][P] \quad (1)$$

where $[L]$ is composed of the significant factors of electrical parameters variation. $[P]$ is a matrix of coordinates in a normalized principal factor space. $[E]$ is a mismatch variation vector of electrical parameters. PFA uses matrix techniques to find orthogonal linear combinations of the measured parameters and quantify the variation associated with each such vector.

The next step is to relate M1 and M2 space to E1 and E2 space by using matrix, $[S]$ of electrical parameters sensitivities to model parameters as expressed in the following equation.

$$[E] = [S][M] \quad (2)$$

By putting equation (1) and (2) equal, we can obtain the solution for $[M]$ in terms of $[P]$ as follows,

$$[M] = [S]^{-1}[L][P] \quad (3)$$

Once matrix, $[M] = [S]^{-1}[L]$ is solved for each device's geometry, linear regression is performed for each matrix element, M_{ij} , which is the model parameter standard deviation, with using the following equation.

$$M_{ij} = \frac{C_{ij}}{(W^{wn_{ij}} L^{ln_{ij}})} \quad (4)$$

where C_{ij} , wn_{ij} , and ln_{ij} are fitting parameters.

3 EXPERIMENTS

We measured mismatch variations of 14 key electrical parameters in FET pairs of different 17 device sizes. Experimental data is from a 90 nm CMOS technology [4]. The key parameters include threshold voltage (V_t), channel current (I_{ds}), transconductance (g_m), channel conductance (g_{ds}) and subthreshold slope (S) over all operational biases. To make the measured parameters unitless, each is normalized by its nominal value from SPICE simulation. The reason of using a simulation value for normalization is to have the equivalent expression of electrical parameter used in both right and left hand side of (1).

We did the PFA independently for each of 17 device sizes. When the correlation matrix is used in PFA, each element of the loading matrix, l_{ij} in (5), generated from PFA represents a relative weight for the j_{th} factor contributed to the total variance of the i_{th} electrical parameter. Using this loading matrix, the matrix, $[L]$ in (1),

is calculated by multiplying a diagonal matrix of the standard deviations of electrical mismatch variations. An example of matrix expression for calculation of $[L]$ is shown in (5).

$$[L] = \begin{bmatrix} \sigma v_t & 0 & 0 & 0 \\ 0 & \sigma i_{ds} & 0 & 0 \\ 0 & 0 & \sigma g_m & 0 \\ 0 & 0 & 0 & \sigma g_{ds} \end{bmatrix} \begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{21} & l_{22} & l_{23} \\ l_{31} & l_{32} & l_{33} \\ l_{41} & l_{42} & l_{43} \end{bmatrix} \quad (5)$$

To model the significant factors obtained from PFA, factors of local fluctuations of electrical parameters are converted to vectors variations of device model parameters such as VTH0, U0, etc. for each device size. These were computed as $[M] = [S]^{-1}[L]$ from (3). Other modeling methods [1]-[2] use electrical parameter variance matrix to solve model parameter variance from (2). Each matrix element, S_{ij} , of $[S]$ is a relative ratio of the difference of electrical parameter to the difference of a model parameter and is calculated as (6)

$$S_{ij} = \frac{(e_i - e_{nom})/e_{nom}}{(m_j - m_{nom})/m_{nom}} \quad (6)$$

where e_{nom} and m_{nom} are a nominal value of electrical parameter and model parameter respectively. The increment of an electrical parameter, $(e_i - e_{nom})$ is evaluated using SPICE simulation. Figure 2 show an example of the sensitivity matrix.

$$\begin{bmatrix} \frac{dV_t}{dvth0} & \frac{dV_t}{du0} & \frac{dV_t}{drdsw} & \frac{dV_t}{det a0} & \frac{dV_t}{dk1} \\ \frac{dI_{ds}}{dI_{ds}} & \frac{dI_{ds}}{dI_{ds}} & \frac{dI_{ds}}{dI_{ds}} & \frac{dI_{ds}}{dI_{ds}} & \frac{dI_{ds}}{dI_{ds}} \\ \frac{dg_m}{dg_m} & \frac{dg_m}{dg_m} & \frac{dg_m}{dg_m} & \frac{dg_m}{dg_m} & \frac{dg_m}{dg_m} \\ \frac{dg_{ds}}{dg_{ds}} & \frac{dg_{ds}}{dg_{ds}} & \frac{dg_{ds}}{dg_{ds}} & \frac{dg_{ds}}{dg_{ds}} & \frac{dg_{ds}}{dg_{ds}} \\ \frac{dS}{dS} & \frac{dS}{dS} & \frac{dS}{dS} & \frac{dS}{dS} & \frac{dS}{dS} \\ \frac{dV_t}{dvth0} & \frac{dV_t}{du0} & \frac{dV_t}{drdsw} & \frac{dV_t}{det a0} & \frac{dV_t}{dk1} \end{bmatrix}$$

Figure 2: An example of sensitivity matrix of model parameters. Vth0, u0, rds, eta0, and k1 are BSIM4 model parameters.

The last step is to model geometric dependence for each matrix element, M_{ij} , of variations vector of the extracted device model parameters across different device sizes. It is described in the previous section. The expression for the i_{th} model parameter distribution is,

$$(\sigma M_i)^2 = \sum_{j=1}^n (M_{ij} P_j)^2 \quad (4)$$

where P_j is a normalized Gaussian distribution with mean at 0 and standard deviation of 1, n is the number of independent distributions which is the number of the most significant eigenvectors.

4 RESULTS AND DISCUSSIONS

From PFA, we identify the three the most significant factors which were common to all geometries and constructed an independent random distribution to model each factor of $[P]$ in (1). For each of the first three eigenvectors the dot products between geometries were near unity, indicating that essentially the same principal factors exist in all geometries. These three eigenvectors explain about 75% of the total variance of electrical parameters. We suggest that these statistical degrees of freedom represent variation in the total dose and in the geometric distribution of dopant in the channel region [5].

Three principal factor variations are modeled using VTH0, U0, RDSW, VSAT, K1, ETA0, DVTP1, and PDIBLC2. To evaluate the accuracy of model, first the correlation coefficients (R^2) are compared. The model predicts the R^2 within 20% except for gmss and gdsm as shown in Table 1. Considering modeling capability of

1x0.08 (WxL)	vtss	vtsl	idsl	idss	gmss	gdsm
vtss	1	0.77	-0.52	-0.79	-0.52	-0.93
vtsl	0.9	1	-0.68	-0.82	-0.11	-0.6
idsl	-0.55	-0.6	1	0.92	0.57	0.57
idss	-0.67	-0.74	0.91	1	0.57	0.81
gmss	-0.11	-0.11	0.63	0.53	1	0.67
gdsm	-0.69	-0.57	0.51	0.64	0.14	1
3x0.4 (WxL)	vtss	vtsl	idsl	Idss	gmss	gdsm
vtss	1	0.98	-0.88	-0.91	-0.79	-0.56
vtsl	0.93	1	-0.81	-0.85	-0.69	-0.13
idsl	-0.71	-0.71	1	0.99	0.98	0.37
idss	-0.79	-0.83	0.89	1	0.97	0.35
gmss	-0.54	-0.59	0.86	0.88	1	0.52
gdsm	-0.41	-0.16	0.26	0.23	0.08	1

Table 1: Correlation coefficient matrix for NFET 1x0.08 (WxL) and NFET 3x0.4 (WxL) device. The gray filled boxes are for raw data and white boxes are for model data. Vtss is saturated V_t , vtsl is linear V_t , idsl is linear I_{ds} , idss is saturated I_{ds} , gmss is saturated g_m , gdsm is g_{ds} at 0.5Vdd.

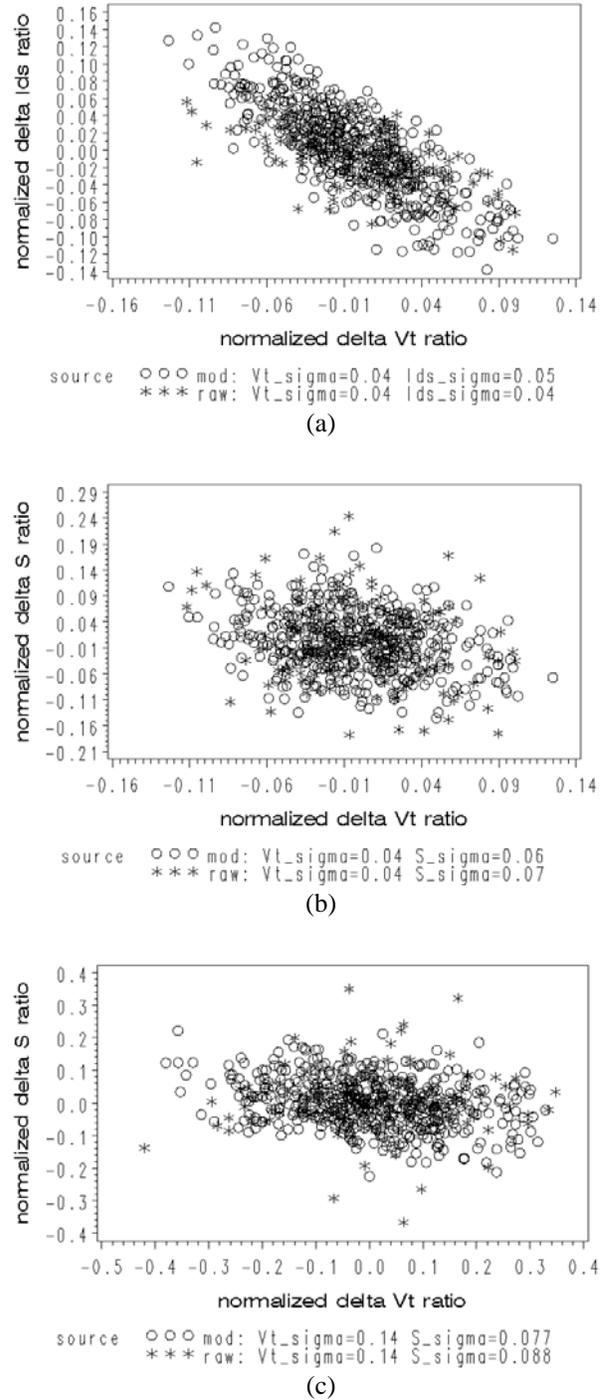


Figure 3: Scatter distribution of normalized mismatch variations. The “mod” (o) is simulation and “raw” (*) is hardware data. (a) Saturated $\Delta I_{ds}/I_{ds0}$ (Y-axis) and saturated $\Delta V_t/V_{t0}$ (X-axis) for NFET 1x0.08 (WxL) device, (b) Saturated subthreshold slope, $\Delta S/S_0$ (Y-axis) and saturated $\Delta V_t/V_{t0}$ (X-axis) for NFET 1x0.08 device, (c) Same plot as (b) for NFET 0.12x0.08 (WxL) device.

BSIM model for g_m and g_{ds} , the result is satisfactory. The scatter plots in Figure 3 are another way of showing correlation in model as compared to hardware.

The dependence of the model on device sizes is shown in Figure 5.

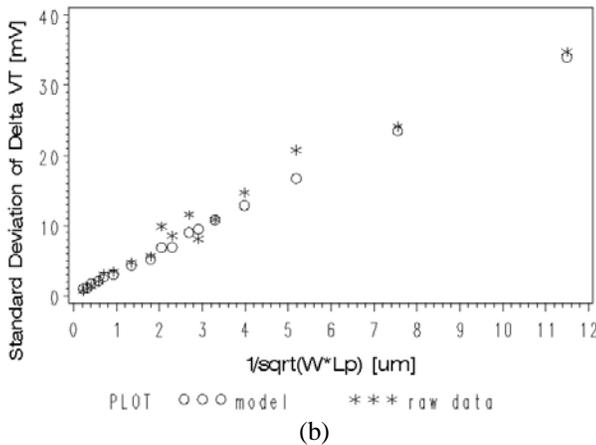
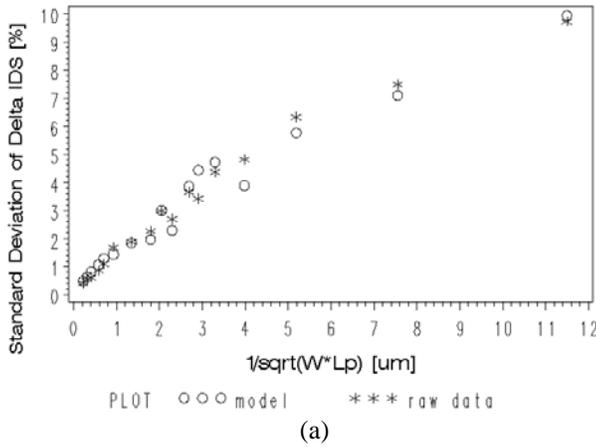


Figure 5: Dependence of mismatch variation on device sizes. The “model” (o) is simulation and “raw data” (*) is hardware data. Y-axis is the standard deviation of (a) delta saturated I_{ds} ratio and (b) delta saturated V_t . X-axis is the square root of device area.

5 CONCLUSION

We propose a new modeling technique able to capture the correlated effects in the local fluctuations of key MOSFET electrical parameters as a function of device size. We found three strong degrees of freedom which may relate to dopant fluctuation in various regions of the device. We demonstrated the accuracy of the model as compared to hardware by evaluating 1) correlation coefficients in electrical parameters and 2) dependence of model on various device sizes.

REFERENCES

- [1] Patrick G. Drennan et al, IEEE J. Solid-State Circuits, vol.38, pp. 450-456, Mar. 2003
- [2] Jeroen A. Croon et al, IEEE J. Solid-State Circuits, vol.37, pp. 1056-1064, Aug. 2002
- [3] Jiri Slezak et al, NSIT-Nanotech 2004, vol.2, pp. 144-146, 2004
- [4] Shih-Fen Huang et al, IEDM 2001, pp. 237-241
- [5] Xinghai Tang et al, IEEE Trans on VLSI System, vol.5, no.4, pp. 369-376, Dec. 1997