Packaging Design with Thermal Analysis of LED on Silicon Substrate

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ABSTRACT

In this paper, we demonstrate a package method for a package component of LED (Light Emitting Diode) using state of the art MEMS technologies and careful materials selection such as using a silicon substrate to dissipate heat and match thermal expansion coefficient (CTE). The objective is to develop an LED package that can overcome LED life, high operating voltage, package degradation and the ability to drive the devices at higher power and higher brightness. To numerically predict the performance of packaging design, the optical and thermal characterization of the novel package structure was evaluated and simulated by TracePro and ANSYS software respectively. Research results have shown that silicon substrate can enhance heat removal for safe junction temperature operation and minimize thermal stress caused by mismatch of CTE.

Keywords: LED package, MEMS, silicon substrate, thermal stress

1. INTRODUCE

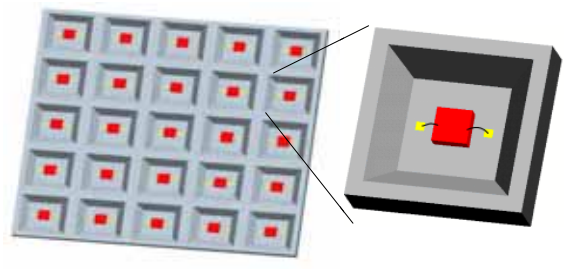
The technology base underlying semiconductor optoelectronics has advanced rapidly over the past decade. For example, light emitting diode (LED) has already begun to penetrate color, and some specialty white, lighting markets. The conventional LED has superior characteristics such as long life time, low power consumption, high contrast, and wide viewing angle. This has resulted in a variety of applications such as full color display, automotive interior, backlight, and traffic signals. With the progress of technology, the request for LED also improves relatively, and let traditional LED meet the great challenge. The application of the conventional LED would provide the high-power and high-brightness for the commercial development. However, today even the most powerful LED being made are still an order of magnitude too low in flux per LED, and two orders of magnitude too high in cost per lumen to significantly penetrate the general illumination market. These problems make the realization of high-resolution, high brightness, high density and low-cost luminous devices or displays difficult. In particular, the typical thermal design problem for a LED system revolves is around the efficiency of LED packaging [1,2].

In the past twenty years, LED used for indicator lamps were packaged in two-lead devices similar in shape to small bulbs. Those packages were placed LED on a metal substrate (Aluminum reflector) and use the highly transparency epoxy encapsulation (lamps) as the seal material. However, the problem is that the high-power LED package the heat generation from conventional LED chips and generation thermal stress from the mismatch of thermal expansion coefficient will be directly effect the package reliability and device fatigue. Consequently, these package methods did not meet to the future high-power LED or/with high density modulus [3,4]. With the continuous improvement in the LED packaging, several packaging method have been approached to improve high-power LED performance. They use the silicon wafer as a micro-reflector to absorb the heat generated by the LED chip, and develop the full color LED display panel using LED array units mounted on a silicon micro-reflector. However, a higher density LED array unit is limited the layout of connected electrodes. In short, each of those approaches has potential advantages and obvious technical challenges [5].

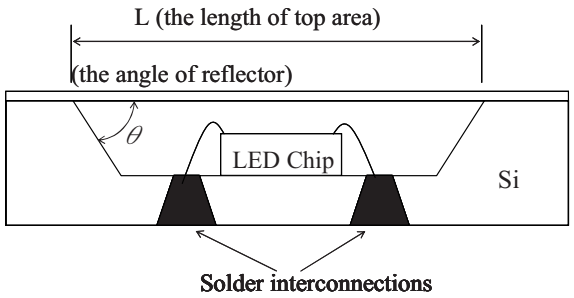
From the above discussion, it is clear that thermal effect and electrodes connection will remain as the key to packaging high-power LED with high density array unit. To solve foregoing problem, we have develop and fabricate a silicon-based packaging platform with metal interconnections for a package component of LED using silicon bulk micromachining and solder ball implantation technologies. The major advantages of the package process are to enhance heat removal for safe junction temperature operation, and minimize thermal stresses caused by mismatch of CTE of which between package substrate and LED chip. To numerically predict the performance of packaging design, the optical and thermal characterization of the novel package structure was also evaluated and simulated by TracePro and ANSYS software respectively.

2. DESIGN

The schematic views of proposed packaging structure are illustrated in Fig. 1. A silicon chip serves as a substrate which is formed with a depression (reflector) and two electrodes guide through holes by means of exposure and development and wet etching. The light emitted from the side of the LED chip is reflected by the tilted (111) surfaces



(a) 3-D



(b) cross section view

Fig. 1 Schematic structures of the proposed packaging.

and the direction of light propagation is upward. The metal interconnections in the depression are to take as positive and negative electrode. The LED crystallite is placed on the base of silicon micro-reflector and connected to the positive and negative electrode by wire bond technique. Then the depression is packaged by glass plate. Finally, the structure is cut along a line between two depressions.

In this design, the substrate is a silicon wafer which has better heat dissipating effect. Moreover, the depression in which the LED crystallite is placed is directly formed in the substrate so that the heat generated by the LED crystallite can be directly dissipated from the silicon substrate to achieve better heat dissipating effect and decrease thermal stresses. Accordingly, the lighting efficiency of the LED can be enhanced. Further, more than two LED with red, green and blue colors of light can be disposed in each metal interconnection. Such structure can achieved a high-density LED array unit and serve as a backlight source of a liquid crystal display panel.

3. ANALYSIS

To study the effect of depression geometry on package performance, full multi-dimensional optical analysis is mad in this research by using computer package TracePro since the light energy of LED is highly depend on the area and angle of tilted surface of reflector. A 3-D model was established, as show in Fig. 2. In which the length of reflector is designed 1.8 mm and the depth is 525 μm. In

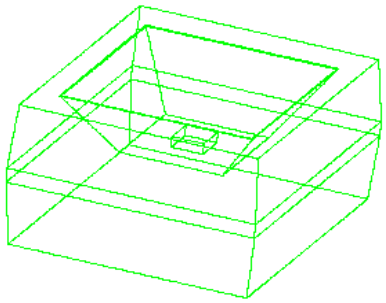


Fig. 2 Established 3-D model for optical analysis.

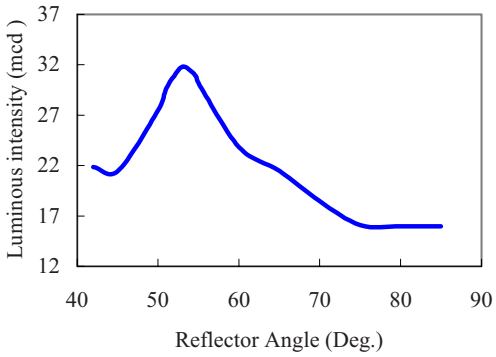
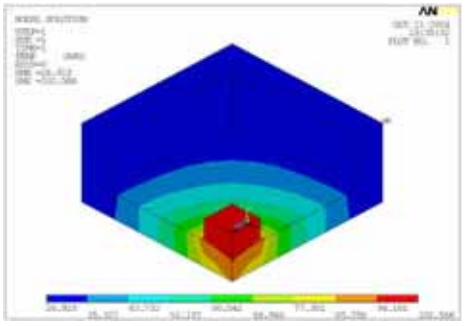
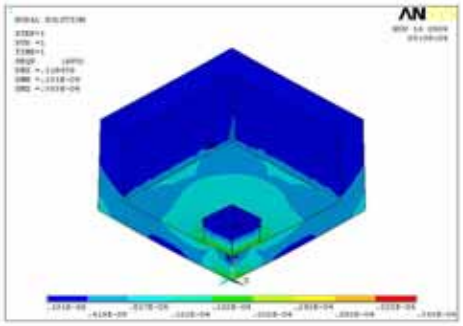


Fig. 3 The variation of the light energy versus reflector angle.

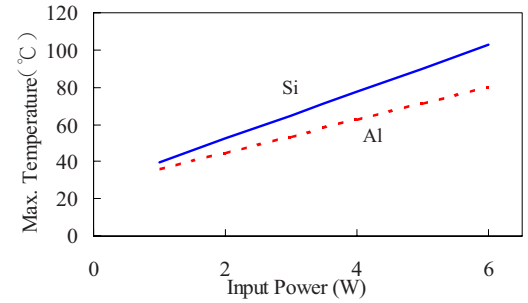


(a) temperature distribution

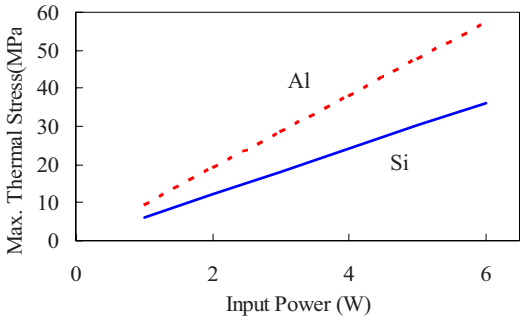


(b) thermal stress distribution

Fig. 4 Typical simulated results of thermal effect.



(a)



(b)

Fig. 5 The variation of the (a) Max. temperature and (b) Max. thermal stress respectively versus input power.

addition, constant luminous flux is set as 0.05 lm. The analysis result of luminous intensity against the variation of reflection angle was shown in Fig. 3. It is seen that a maximum luminous intensity existing at the reflection angle of 53 degree and the value is 32 mcd. With regard to the reflector with the etching angle 54.74 degree, the value of luminous intensity is approximately 31 mcd. That mean the silicon reflector developed can be used to achieve a high brightness.

The thermal effect on the component of silicon substrate within a LED die attached was also simulated using ANSYS software. The geometry of the finite element model is close to a typical LED device. The square length of the LED crystallite is 400μm, while the thickness is around 150 μm. In additional, the reflector is 1.625 mm in square length with a height of 350μm. A heat flux of 3.75×10^{-5} (W/μm^2) is then applied at the LED crystallite that is mounted to the Si substrate. The temperature distribution and thermal stress of analyzed results are respectively shown in Fig.4(a) and 4(b). In which, the maximum temperature and thermal stress were occur on the interface of between LED crystallite and Si substrate. According to the above-mentioned simulation method, the maximum temperature and thermal stress for both silicon and Aluminum reflectors of which applied various heat flux were also determined, as show in Fig. 5(a) and 5(b). Fig. 5 has shown a higher temperature and a lower thermal stress in the silicon reflector case. The thermal stress of Aluminum substrate is approximately 1.5 times more than that of silicon case. It is clear that using the novel packaging design of silicon substrate can sufficient absorbs the heat generated by the LED chip and improves their thermal reliability.

4. FABRICATION AND RESULTS

The silicon-based packaging platform for LED presented in this paper was fabricated by standard bulk micromachining. The basic fabrication process flow is described in Fig. 6. The process starts with a <100> double-side polished p-type silicon wafer (Fig. 6a). At first, the single-crystal silicon chip being placed in a furnace and thermally oxidized to grow a layer of silicon dioxide on the surface of the single-crystal silicon wafer as etching-protective layers (Fig. 6b). Then, the oxide layer is patterned (mask#1 and mask#2) to define the etching regions of the upper and lower faces of the silicon wafer (Fig. 6c). The protective layers within the etching regions being etched by means of wet etching (BOE) to expose the etching regions of Si to outer side (Fig. 6d). After that, by means of non-isotropic wet etching (KOH), the etching regions being etched to a certain depth so as to simultaneously form a reflector in the silicon wafer and at the same time form two through holes on the bottom (Fig. 6e). Finally, conductive

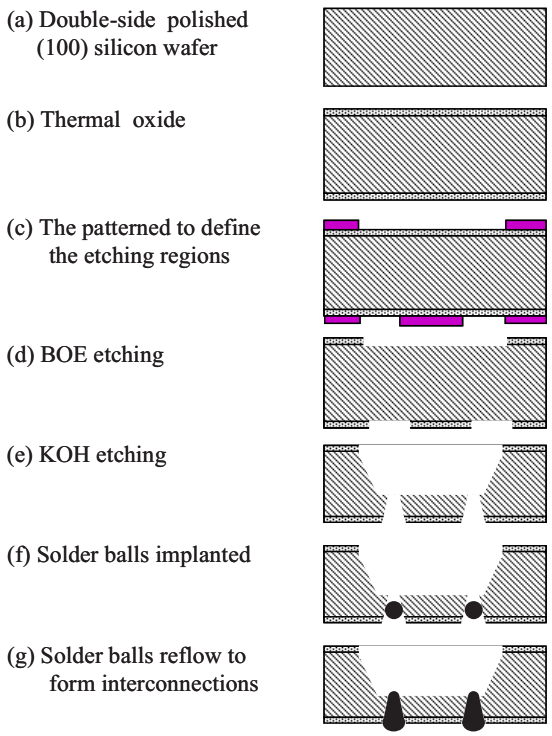
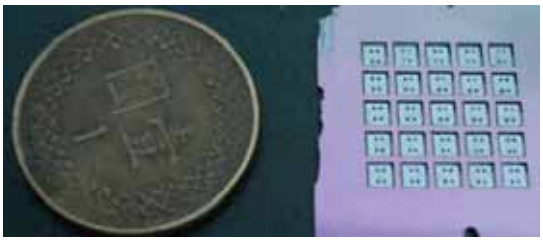
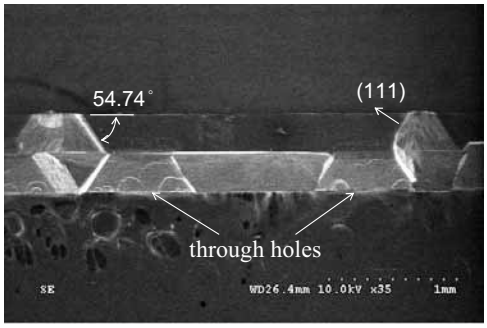


Fig. 6 Fabrication processes flow of the Si-based packaging platform.



(a) 5×5 reflector array unit



(b) cross section view of single reflector

Fig. 7 Photo images of silicon-based reflector.

materials such as tiny solder balls (or conductive glue) being respectively implanted into the through holes of the bottom (Fig. 6f). In this embodiment, the conductive materials being solder balls with the diameter of 600 μm, the substrate being placed into a baker and heated to soften the solder balls and fill up the through holes (Fig. 6g).

After going through the above fabrication processes, the silicon-based reflector is shown in Fig 7. The length L of the square reflector is 3 mm and the depth is 310 μm. Besides, due to the fact that etching in KOH proceeds in silicon at a higher etch rate on higher order planes, such as the <100> plane as compared to the <111> plane, this creates etching at a 54.74 degree angle from the horizontal, as illustrated in Fig. 1(b). The SEM diagram of the etching holes and interconnection that had fabricated is shown in Fig. 8. As shown in Fig. 8, the solder ball was successfully fill up and slightly protruding from two ends of a through hole, whereby when the silicon-based substrate is fixed on the circuit board and the LED had mounted on it, the solder balls contact with the electrodes of the LED and the electrodes of the circuit layout card so as to achieve electrically connection and signal control.

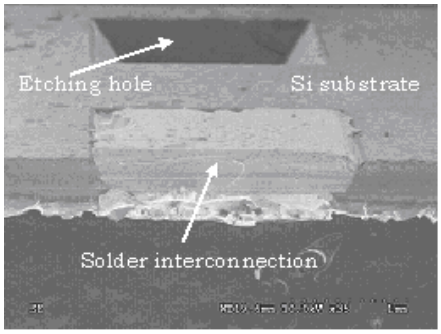


Fig. 8 The SEM image of the packaging platform.

5. CONCLUSION

A novel silicon-based packaging platform with metal interconnections has been developed for packaging optoelectronic semiconductor devices, such as LED. The optical/mechanical characteristics and fabrication processes were evaluated and experimented, and was found practically applicable. Due to the fact of the silicon and LED crystallite has similar CTE and silicon submounts allow integration of a wide variety of electronics, this packaging structure that fabricated by silicon bulk micromachining can be used to effectively improve the reliability and thermal fatigue of high power LED package. Moreover, a high density LED array unit for used LED display panels can be realized at a low production cost because a batch process can be used to fabricate the LED array units.

6. ACKNOWLEDGMENTS

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REFERENCES

[1] M. Arik, J. Petroski, and S. Weaver, “Thermal challenges in the future generation solid state lighting applications: light emitting diodes”, ITHERM 2002, San Diego, California, pp. 113-120, May 2002.

[2] S. Haque, D. Steigerwald, S. Rudaz, B. Steward, J. Bhat, D. Collins, F. Wall, S. Subramanya, C. Elpedes, P. Elizondo, and P. S. Martin, “Packaging challenges of high-power LEDs for solid state lighting”, IMAPS’3, Boston, MA, pp.100-105, November 2003.

[3] K. Hatada, H. Fujimoto, T. Ochi, and Y. Ishida, “LED array modules by new technology microbump bonding method,” Components, Hybrids, and Manufacturing Technology, Vol. 13, pp. 521–527, 1990.

[4] N. Narendran, Y. Gu, J. P. Freyssinier, H. Yu, and L. Deng, “Solid-state lighting :failure analysis of white LEDs,” Journal of Crystal Growth, Vol. 268, pp. 449-456, 2004.

[5] K. Takahashi, N. Tadokoro, and S. Takeuchi, “High density LED display panel on silicon microreflector and integrated circuit,” Electronic Manufacturing Technology Symposium, Omiya, Japan, pp. 272-275, Dec. 1995.