A Nano-Transistor with a Cavity

C. Ravariu*, A. Rusu*, M.D. Profirescu* and F. Ravariu**

*"Politehnica" University of Bucharest, Faculty of Electronics, Splaiul Independentei 313, Bucharest Romania, cristir@mcma.pub.ro
**Institute for Research and Development in Microtechnologies, Romania, florinar@imt.ro

ABSTRACT

A SOI nanotransistor with a cavity was proposed. The global current is a superposition of a tunnel current through the cavity and an inversion current at the film bottom. The tunnel source-drain current prevails in sub 1-nm film thickness and provides the I_D-V_{DS} characteristics with a minimum. For film thickness comprised between 200-10nm, the I_D-V_{GS} curves preserve similar shapes with a classical MOS/SOI's transfer characteristics. For sub 1-nm film thickness, the shape of the I_D-V_{GS} characteristics with a maximum suggests a SET like conduction. From the electron concentration simulations, a transport of the electrons one-by-one in the transistor body result, corresponding to the Single Electron Transistor principle.

Keywords: SOI-MOSFET, SET, tunnel current, simulations, nanodevice

1 INTRODUCTION

The SOI structures represent a possible manufacturing technique for nanodevices, [1, 2, 3]. A uniatomic semi-/conductor layer could be placed onto an insulator support since to be handled and to avoid the leakage through substrate.

In this paper the starting point was a standard SOI-MOSFET, 200nm Si-film on 400nm Oxide. The $I_D(V_{DS}, V_{GS})$ curves were studied for thinner films: 10nm, 1nm, 0.3nm. For sub-10nm film thickness, a new nanostructure, was proposed. The source and drain regions consist in two high "undulations" of Si-n^+ (y_{n+}=7nm) onto an oxide support. The Si-p transistor body was thinned firstly to y_{film}=1nm and secondly to y_{film}=0.3nm. The carriers transport was confined at the limit, one by one. Essentially, the device could be regarded as a string of "Few Electron Transistors" that converges to the "Single Electron Transistor", as an ideal limit. Another reason for two prominent n^+ - undulations is related to the practical possibility of Source and Drain metallization. On the other hand, both thick parallelepiped n^+ - layers fulfill the electron reservoir role, like in a SET case [4].

2 THE NANO-DEVICE DESCRIPTION

The device architecture, presented in fig.1, was inspired from a real sub-10nm undulated polysilicon film, [3]. We preserved just two high parallelepiped shape "undulations" of Silicon onto an oxide support. The source and drain regions are n^+-type silicon ($N_D=10^{17}cm^{-3}$) with z_{n+}=6nm, y_{n+}=7nm, x_{n+}=3nm, placed at x_c =3nm distance. A thinner p – type Si film ($N_A=5\cdot10^{15}cm^{-3}$) links the source and drain regions and represents the inversion channel location. All these parameters will be maintained constant during the simulations. Thinning the p-type film to y_{film}=1nm, than to 0,3nm, a cavity carried out between source and drain. The cavity could be optional covered with an oxide layer (not presented in fig. 1, but presented in simulations). However the vacuum properties are fulfilled in nanocavity.

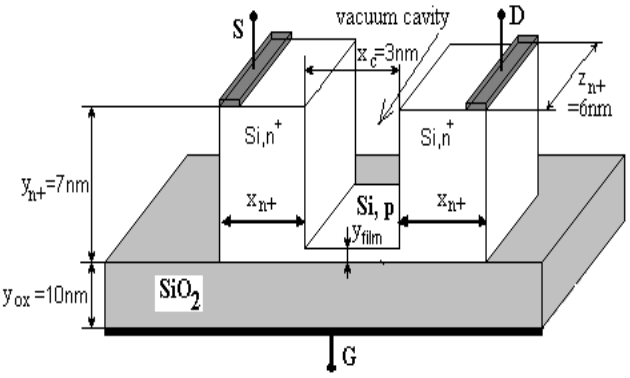

Figure 1: The basic structure of the SOI nanotransistor.

The device body is placed onto an oxide layer (y_{ox}=10nm). The substrate contact acts like a gate terminal. Because the vacuum distance is less than 4nm (x_c<4nm), then the probability of tunneling between n^+ - source to n^+ - drain meaningfully increases, [5].

3 AN ANALYTICAL STUDY

A specific nanodevice phenomenon, the tunnel effect through a triangle potential barrier, occurred. Some electrons tunnel the Si - Vacuum barrier, producing the tunnel current, I_t [5]:

$$I_t = \frac{A}{\sqrt{E_b}} \cdot \left(\frac{V_{DS}}{x_c}\right)^2 \cdot \exp\left(\frac{B \cdot E_b^{3/2} \cdot x_c}{V_{DS}}\right) \qquad (1)$$

where $E_b = \chi_{semic} - \chi_{vacuum}$ is the height of the triangle barrier of the potential from semiconductor to vacuum and A, B are some material parameters depending on the effectiveness mass for electrons and holes, [5]. Zeroing the first order derivative of the model (1) results a minimum for the tunnel current versus V_{DS} voltage:

$$V_{DS}\big|_{I_t=min} = \frac{B \cdot E_b^{3/2} \cdot x_c}{2} \qquad (2)$$

The simulations proved that the total current presented this curvature with a minimum when the film thickness decreased under 1nm because the percentage of the tunnel current, I_t overcomes that from the inversion channel, I_{MOS}, fig.2. For thicker Si-p film (y_{film}>10nm), the tunnel current is negligible and the characteristics tends to those of the classical SOI-MOSFET. The cavity itself has a high vacuum. The number of air molecules N, in the cavity volume for y_{film}=1nm, is:

$$N = \frac{x_c \cdot (y_{n+} - y_{film}) \cdot z_{n+} \cdot N_A}{V_{m0}} \approx 2{,}8 \text{molecules} \qquad (3)$$

Consequently, the electrons weren't disturbed by the air from the cavity, in normal conditions (N_A=6,023×10^{23}molec/mol, V_{m0}=22,42dm^3/mol). So, the device doesn't require a special vacuum technology.

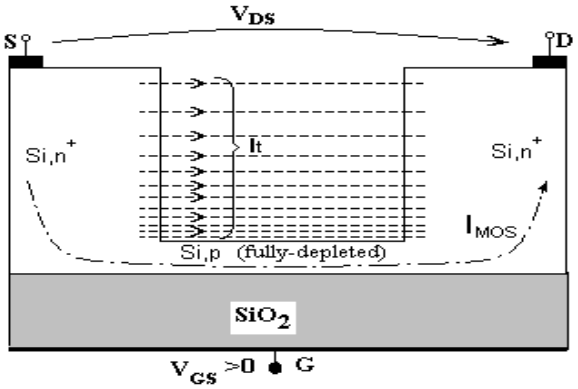

Figure 2: The current flow in a cross-section.

4 THE SIMULATION RESULTS

In the simulations with ATLAS, the constructive data were those described in paragraph 2. The "nano-effects" were simulated using ATLAS, taking into account the: Band to Band Tunnelling, Fowler-Nordheim tunnelling, Fermi distribution, including in the MODEL statement the following parameters: BBT, FNORD, FERMI. For comparisons, the voltages were the same: V_G= 0V…3V, V_D=0V…4V, V_S=0V, for all structures. The film thickness was varied. The simulations begun with a standard SOI 200nm Si / 400nm Oxide. Figure 3, 4 presents the potential distribution and the electron concentration in the structure with 200nm film thickness. A positive gate bias induces an electron inversion channel in p-type film (e.g. $n\big|_{y=0.2um} = 10^{16}\,cm^{-3} > 5 \cdot 10^{15} cm^{-3} = N_{A\text{-}film}$), fig.4.

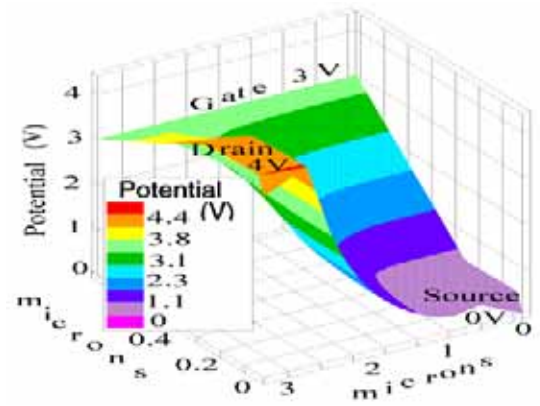

Figure 3: The potential distribution in the 200nm structure.

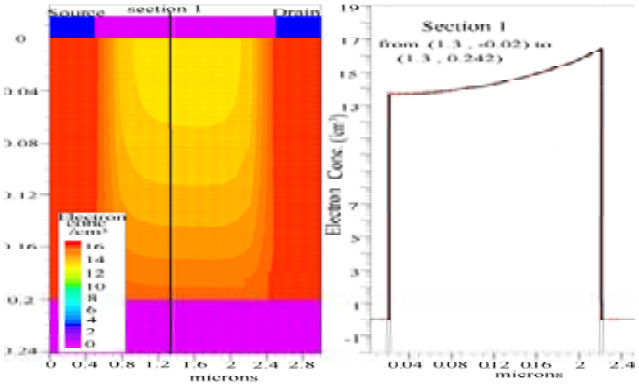

Figure 4: The electron concentration in the 200nm structure, detail in the film.

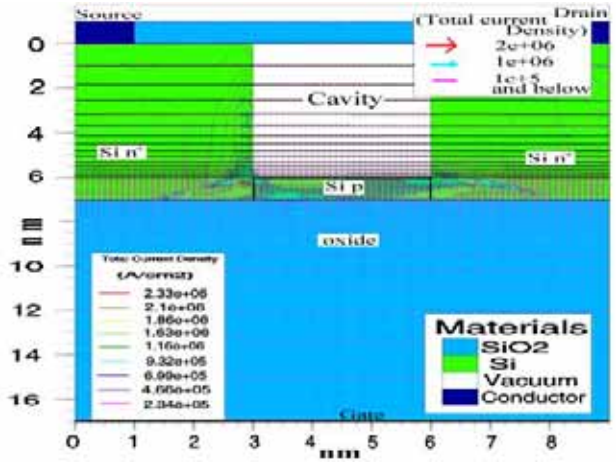

Figure 5: The current flow through the 1nm structure.

The current vectors through the vacuum proved the tunnel effect in the cavity, (black dots in fig. 5) for the nanotransistor with y_{film}=1nm and cavity, at V_D=4V.

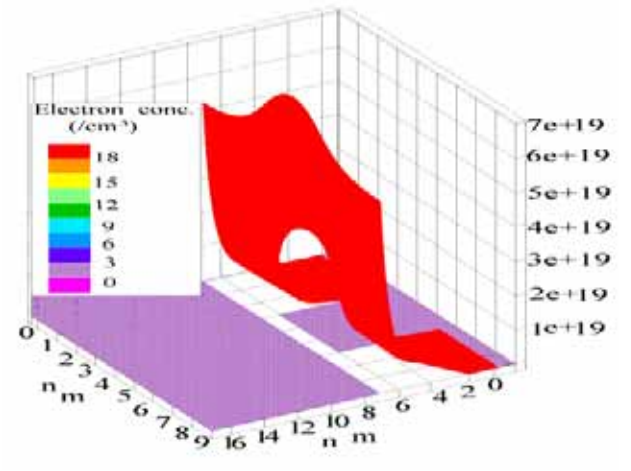

Figure 6: The electron concentration in the 1nm structure.

The electron concentration from fig.6 reaches a maximum about $6 \cdot 10^{19} cm^{-3}$ in the middle of the inversion channel, proving a strong inversion onset, at V_G=3V.

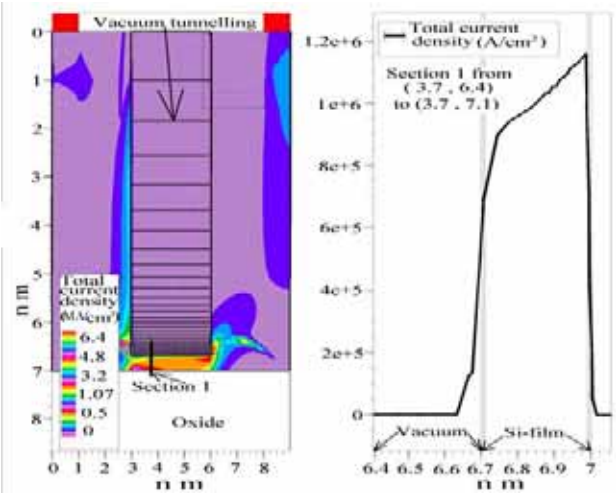

Figure 7: The total current density in the 0.3nm structure.

Despite of the very thin p film, (y_{film}=0.3nm), a high electron concentration occur in the channel at V_G = 3V. As is shown in fig.7 the I_{MOS} current prevails. The conduction between S – D is ensured through the inversion channel. When V_{DS} increases, the current I_t arises, as a superposition, because the vacuum between source and drain is tunneled. Figures 8 and 9 comparatively present the simulated static characteristics for all the structures, after ATLAS running. In fig.8 the family of I_D-V_{DS} curves at V_{GS}=3V, for y_{film}=200nm, 10nm, 1nm, 0.3nm is presented. These curves with a minimum prove the tunnel current involvement, accordingly with the equations (1, 2).

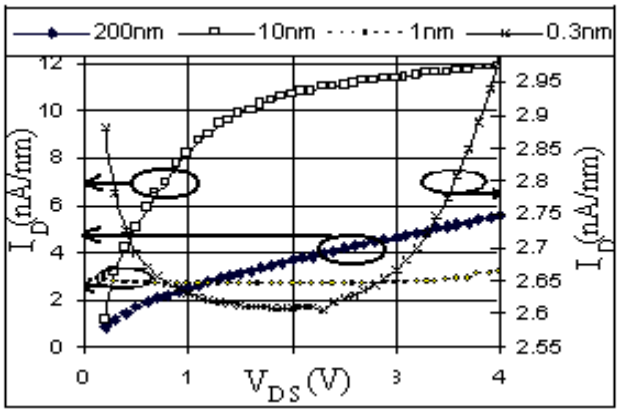

Figure 8: The I_D-V_{DS} characteristics, at V_{GS}=3V.

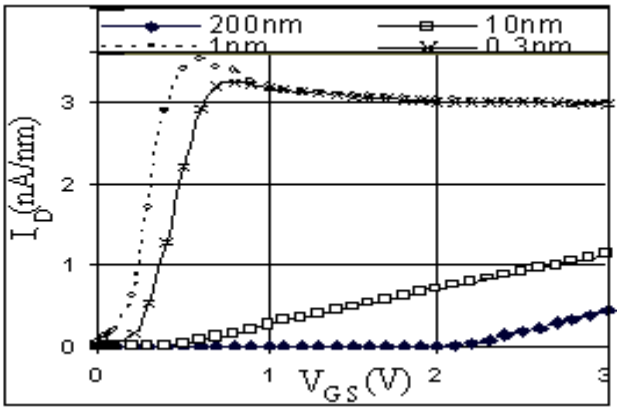

Figure 9: The I_D-V_{GS} characteristics, at V_{DS}=0.1V.

For I_D–V_{GS} transfer characteristics from fig.9, the drain voltage was 0.1V, and the gate voltage was increased from 0V to 3V with a 0.05V step. Special characteristics with maximums appeared just for the nanotransistors with cavity.

However the device is in strong inversion at this gate voltage, because $n_{channel} > 10^{19} cm^{-3} >> 5x10^{15} cm^{-3} = N_{A\text{-}film}$, fig.10.

5 A SET LIKE BEHAVIOUR

ATLAS simulations proved the SET like behavior of our SOI nanotransistor with a cavity.

Figure 10 presents the electron concentration in 0.3nm structure (uniatomic Si layer) at V_{DS}=0.1V, V_{GS}=3V, when a strong inversion occurs. The electron concentration in the middle of the channel is: $n = 2 \cdot 10^{20} cm^{-3} = 0{,}2 nm^{-3} \approx 1$electron per channel volume, V ($V = y_{film} \times x_c \times z_{n+} = 0{,}3nm \times 3nm \times 6nm = 5{,}4nm^3$). This means that the electron transfer in the uni-atomic Si layer is one by one. Hence, the behavior of this ultra thin SOI nanotransistor with a cavity is similar to a SET device.

Another reason to associate these transistors is given by the transfer characteristics from fig.9, for y_{film}=1nm and 0.3nm, having a maximum, like SET [4].

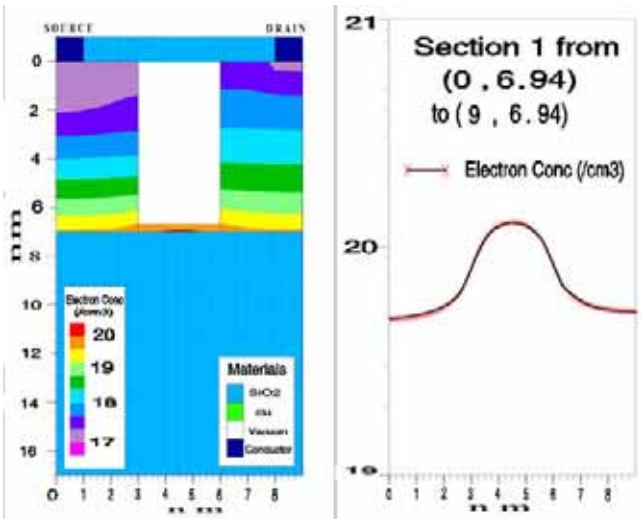

Figure 10: The electron concentrations in 0.3nm structure.

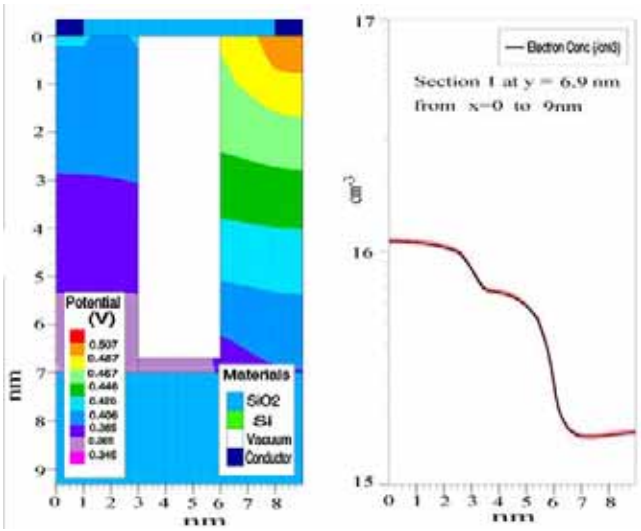

Figure 11: Potential and electron concentration in 0.3nm structure.

Figure 11 present the global potential distribution (left) and a detail of the electron concentration (right) for the 0.3nm structure with cavity, biased at a high drain voltage in this last case (V_S=0V, V_G=3V, V_D=4V). The same voltages were applied in fig.7, where the tunnel current density attained just $7 \cdot 10^5 A/cm^2$, while the MOS current density reached to $1.2 \cdot 10^6 A/cm^2$. This proved that the tunnel component significantly exists, but less than the inversion channel current, that give the SET like behavior. In this case the saturation occurred and an unbalanced electron distribution can be seen in the film (fig.11): $1.1 \cdot 10^{16} cm^{-3}$ in the source region, $7 \cdot 10^{15} cm^{-3}$ in the channel near the source, $2 \cdot 10^{15} cm^{-3}$ in the channel near the drain and decrease up to $1.4 \cdot 10^{15} cm^{-3}$ in the drain region, at the film bottom.

6 CONCLUSIONS

A sub 1-nm SOI nanotransistor present quantum effects (e.g. I_D-V_{GS} with a maximum like the SET transistor). The shape of the ID-VDS curves with a minimum proves the presence of the tunnel effect. Also the electron transfer in the uni-atomic Si layer is one by one as in a SET transistor. The nanocavity comprises 1-3 air molecules in normal conditions, negligible for current transport. Consequently doesn't imply special vacuum technologies. This structure could be a possible method to manufacture a SET variant.

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