

# Investigation of Robust Fully-Silicided NMOSFETs for Sub-100 nm ESD Protection Circuits Design

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## ABSTRACT

This paper demonstrates a fully-silicided ESD protection device design in sub-100nm integrated circuits. No drain ballast resistor required is the most significant feature that makes the new device differ from the conventional ones. Accordingly, a simplified manufacturing process and a reduced device area could be obtained simultaneously. It is believed that the achievements are caused from the floating charge effects during the ESD stressed. On the other hand, in avoiding the device function affected by the floating charges, a switch is incorporated at the body electrode. The newly designed device structure is very attractive in novel ESD design for the consideration of its low cost, small size and high efficiency.

**Keywords:** Fully-silicided, ESD protection, floating body design, thin gate-oxide, turn on voltage, turn on resistance, efficiency

## 1 INTRODUCTION

Electrostatic discharge (ESD) has long played an important role in integration circuit design; in roughly estimating, ESD responses for several percents of the chip failure in modern VLSI manufacturing [1-12]. Accordingly, how to design a robust ESD protection circuit with a high efficiency is an important issue for IC designs [1-2]. Traditionally, in having a strong ESD protection circuit, the drain ballast resistor made from the non-silicided diffusion region has been placed between the drain contacts and polysilicon gates [3-6]. However, it requires an additional photo-mask, enlarges the devices area, and an extra device models in VLSI circuit design. The consequence will make a higher process cost, a lower devices density, and a poorer circuit performance. Therefore, a fully-silicided MOSFET device is a good choice in ESD protecting circuits. Unfortunately, it suffers a low ESD robustness [7-10], especially for the sub-100nm era.

In this paper, we propose a novel device structure to improve ESD robustness of fully-silicided MOSFETs. This alternative lets the body electrode in floating state under

ESD stress. The experimental results show that the floating body devices reduce the turn voltage, improve the ESD performance, and have a better robustness for sub-100nm device design. The test devices are fabricated with standard CMOS process with a 90 nm lengthen gate and a 1.2 nm thicken gate-oxide. The ESD characteristics are verified with the Barth model 4200 TLP systems with a pulse width of 100 ns. It can be found that the body floating one has a much better ESD robustness than the body grounded one. The improvement could be caused from the impact ionization holes that accumulate and built up an electrostatic potential at the substrate; consequently, decrease the turn on voltage of parasitic BJT. A decrement of turn on voltages will suppress the damage of gate oxide and reduces the drain electric fields. We can also indicate that there is a wider current path existed in the body floating devices, as a result, the device sustains a better ESD strength than the grounded body one does.

We have presented a constructive alternative for designing a fully-silicided ESD protection device. It exhibited an excellent efficiency on both protection and chip area, and is attractive to sub-100 nm CMOS circuit era.

## 2 DEVICE FABRICATION AND MEASUREMENT

The test devices were fabricated by using a standard twin well CMOS process. The minimum gate length of this process is 90nm and the thickness of gate-oxide is 1.2nm. Cobalt silicide has long been used in deep sub-micrometer devices for its high thermal stability and low resistance in narrow width silicide line. Thus, in our experiments, a 20 nm thicken cobalt silicide is formed by using two steps rapid thermal process in exploring the fully-silicided ESD protection devices.

Interconnections were achieved by copper line and low dielectric constant (low K) insulator. The ESD characteristics were verified by using Barth model 4200 TLP system shown in figure 1, which generates a pulse wave with a width of 100 nano-second. Comparing with experimental results, the measured result is reflected to the human body model (HBM) value.

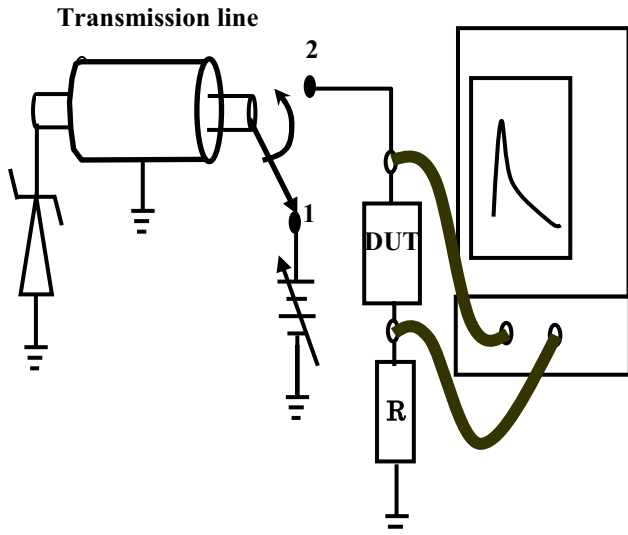


Figure 1: An illustration of the TLP measurement configuration in the study.

### 3 RESULTS AND DISCUSSION

Drain ballast resistor is the most used design methodology for ESD protection devices. The main purpose of the design is altering the current flow path at the drain junction. Make it more clearly that, with adding the resistor, the currents will prefer flowing through the deep junctions instead of drain extensions. The ESD current flowing through the deep junctions will take many benefits:

1. Extensions are much shallower than the deep junctions that confining current flowing in a very narrow path. Thus, current flowing through the deep junctions will result in a much wider path, cause a lower current density and sustains a better ESD robustness; and
2. The current paths at the deep junctions will reduce the electric field and the hot carrier at the channel region of the MOSFET; consequently, the gate-oxide damage from the hot carriers will be greatly reduced.

Conventionally, the ballast resistors are achieved by using a photo-mask that removes all the silicide on this region. The process will produce a non-silicided region that provides a ballast resistor at drain side. The ballast resistor, however, causes two main problems in designing of ESD protection devices. First, the non-silicided region will occupy a large area, for the most designs, the resistor dominates more than one half of the protection device. This result could be easily obtained from the comparison between Fig. 3 and Fig. 5. Second, the resistor will increase the turn on resistance of the protection devices; therefore, make the core circuits have a higher risk from ESD damages. According to previously discussion, a fully silicided ESD protection device is greatly preferred by all the circuit designers. Unfortunately, it is well known that the structure suffers a weak ESD robustness. The result, in

our theoretical analysis is only true for normally used body grounded MOSFETs but not for the floating ones. The layouts of those two structures are presented in the Fig. 3 and Fig. 4 respectively; moreover, the schematics are also shown in the Fig. 2 (a) and 2 (b) below.

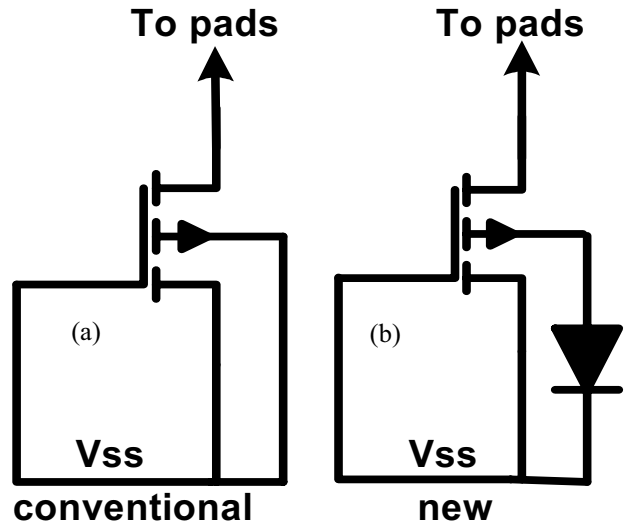


Figure 2: The schematics of the fully-silicided NMOSFET with (a) body grounded (b) Floating body.

Figure 6 presents the IV characteristics measured from the TLP. A clear result could be found that the floating body one has a much better ESD robustness than the grounded one. The results are highly matched with our theoretical predicted results.

The improvement could be due to an accumulation of impact ionization holes at substrate, which decrease turn on voltage of parasitic BJT. Owing to a decrement of turn on voltage, the damage of gate-oxide could be suppressed and the drain electric field could be also lowered. Moreover, for the body floating devices, a wider distribution of current flowing paths will keep away from the channel interface that could also enhance the ESD strength. Thus, the floating body one not only has a lower temperature distribution, but also prevents gate-oxide from hot carrier damage. On the other hand, the grounded body one has a much narrower distribution of current paths that located much closer to the gate-oxide interface. The current distribution not only produces a higher temperature distribution but could also have a risk of gate-oxide damage.

The novel ESD protection structure proposed in this experiment has been demonstrated having a superior ESD robustness. In comparing with the TLP IV characteristics of the normally used partially silicided and our proposed fully-silicided ESD protection devices in the Fig. 7, it could be found that the fully-silicided one has a much lower turn on resistance and a lower turn on voltage. Similar results could be made from the observation of Fig. 8 that an increment of the non-silicided width will result in a higher turn on resistance. Owing to those two characteristics, the voltage dropping through the gate-oxide of the input stage will be

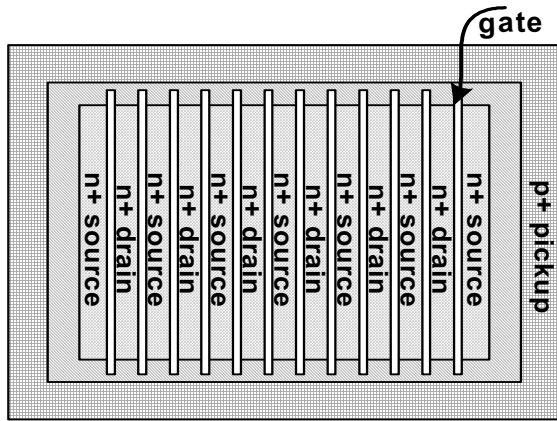


Fig. 3. Top view of the conventional fully-silicided multi-fingers device.

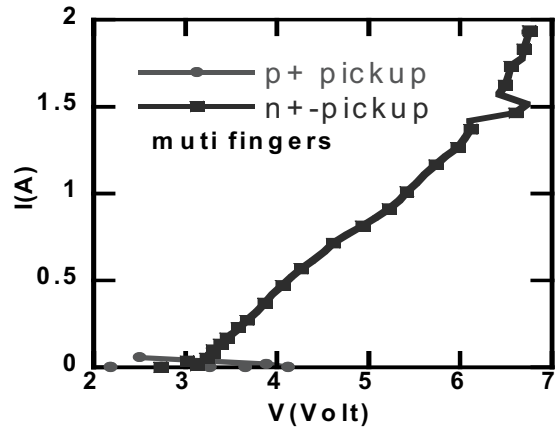


Fig. 6. The TLP measured IV curves of the two fully-silicided devices ( $W=320\mu\text{m}$ ).

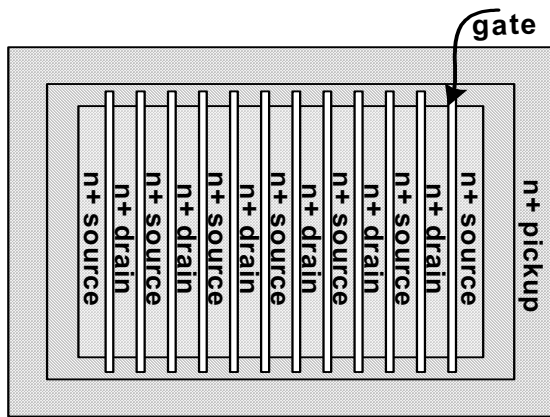


Fig. 4. Top view of the new fully-silicided multi-fingers device.

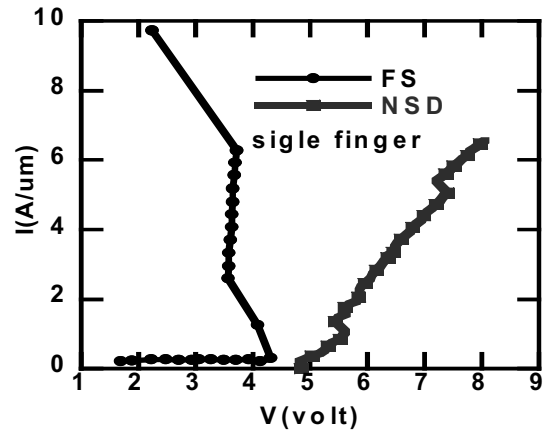


Fig. 7. The TLP measured IV curves of the new fully-silicided and the conventional silicide blocked devices ( $W=20\mu\text{m}$ ).

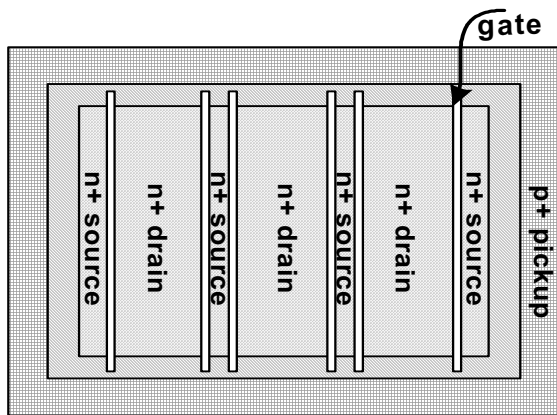


Fig. 5. Top view of the conventional silicide blocked multi-fingers device.

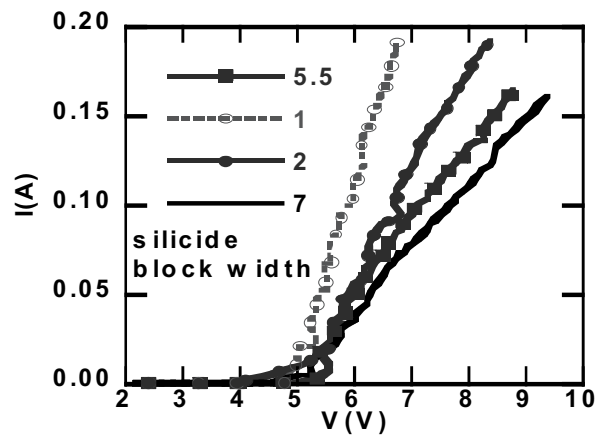


Fig. 8. The TLP measured IV curves of the conventional silicide blocked devices with different block width.

largely reduced. Those features are greatly helpful for keeping the core circuit away from ESD damages. Furthermore, in our experiences, the drain ballast resistances occupied over one half area of the device; thus, in comparing with the normally used ESD protection device, the fully silicided devices save over fifty percents of the area.

The fully silicided structure has been also tested in the whole chip circuit design. It is found that the benefit of the floating charge effects would not be eliminated due to the common substrate. This result is mainly caused from the fact the common substrate is too inefficient to pick the hole out from the well region.

It could be further addressed that the earlier turn on characteristics is actually a very wonderful property in protecting the ultrathin gate-oxide devices. Owing to the drain ballast resistor cannot lower the turn on voltage of the protection device; the device could have a gate-oxide breakdown earlier than the parasitic breakdown. When this situation occurred, the drain ballast resistor is not functional. Here, we can make a brief summary that the floating body fully silicided structure has a very high efficiency in saving the chip area and protecting circuit from ESD damage. It is especially useful in the ultrathin gate-oxide devices.

#### 4 CONCLUSIONS

We have presented a constructive alternative for designing a fully-silicided ESD protection device. It exhibited an excellent efficiency on both protection and chip area, and is attractive to sub-100 nm CMOS circuit era. Floating body fully silicided MOSFET devices have been explored and demonstrated a good ESD robustness in this paper. Those devices have a lower turn on voltage, a lower turn on resistance, a good ESD robustness, and a high efficiency in both the area usage and protection. It is very attractive in novel ESD protection circuit design, especially suitable for ultrathin gate-oxide devices design. For example, the sub-100nm CMOS integration circuit designs.

#### 5 ACKNOWLEDGEMENTS

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