

A Unified Mobility Model for Excimer Laser Annealed Complementary Thin Film Transistors Simulation

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ABSTRACT

In this paper, a unified SPICE mobility model for excimer laser annealed lower temperature polycrystalline silicon (LTPS) complementary thin film transistors (TFTs) is proposed. In comparing with the conventional RPI model, the proposed mobility model exhibits very good property in representing the vertical electrical field induced mobility degradation. Our model improves the correctness of the circuit simulation without increasing any complexity and having no any convergence issue. Comparisons among the conventional RPI TFT mobility model, and measurement data, this new mobility model demonstrated very good accuracy in the simulation of laser annealed LTPS TFTs. This TFT model is very useful in precisely modeling the circuit characteristics for the complementary system on panel (SOP) circuit.

Keywords: excimer laser annealed, LTPS, complementary TFT mode, SPICE mobility model, gate induced mobility degradation.

1 INTRODUCTION

Excimer laser annealing technique has recently been proposed in the fabrication of low temperature polycrystalline silicon; in particular for the applications to active-matrix liquid crystal display (AMLCD) [1] and achieving system on panel. In comparing with the traditional thin film transistors, the most attractive property of the laser annealed polycrystalline silicon is due to its relatively larger grain size and higher electron-hole mobility. Therefore, the embedded driving circuit could be easily achieved for replacing the additional driving integration circuits (IC's) in LCD's. It is known that circuit models play important role in the design of the embedded driving circuit using laser annealed LTPS TFTs. Unfortunately, most of mobility models are valid only for some conventional TFTs and can not be applied to the

simulation of the laser annealed LTPS TFTs [2-3] accurately.

In this work, we propose a unified mobility model which is suitable for the simulation of both the n- and p-type laser annealed LTPS TFTs. This unified mobility model for complementary TFT devices is successfully developed, verified and implemented in the SPICE circuit simulator. By considering the channel mobility degraded by the vertical electric field, this empirical model is similar to the BISM4-liked MOSFET mobility model. With the well-known RPI TFT model, this mobility model can be directly incorporated into SPICE circuit simulator without any convergence problems. To test the accuracy of this new RPI TFT model, we firstly apply genetic algorithm to optimize it with the measured I-V data. This intelligent model parameter optimization methodology has been successfully developed by us in HBT characterization recently [4]. Therefore, a set of characterized model parameters can be extracted precisely. Comparison with the conventional model is also performed on different TFTs [5-7]. Simulation and measurement results for the n- and p-type laser annealed LTPS TFTs are reported and discussed in this work. It is found that simulation with our model demonstrates very good agreement with the measurement. The improvement is unified for both the n- and p-type laser annealed LTPS TFTs. The driving circuit designed with the complementary TFTs is known to have a lower leakage current, and then extend the battery lifetime of the personal data assistant. Thus, this result is very promising and useful in designing the driving circuit by complementary TFTs.

Section 2 discusses the fabrication and measurement procedure for the test devices. In section 3, we state the conventional RPI TFT model. Section 4 reports the

proposed TFT mobility model. Comparison results are discussed in this section. Section 5 is focus on the model parameter extraction and accuracy issues. In section 6, we apply the model to simulation n- and p-channel TFT. Section 7 draws the conclusions and suggests the future works.

2 DEVICE FABRICATION AND MEASUREMENT

The complementary TFTs are fabricated on the glass substrate by using the novel excimer laser annealing process. A 50 nm thick amorphous silicon film is firstly deposited by using a PECVD cluster tool at 300°C. The silicon film was then taken into a novel excimer laser system to transform the amorphous silicon into the large grained poly crystalline silicon. The key process will improve the mobility of both electrons and holes.

After the source/drain formatted by using the high power plasma implantation, a 100 nm thick oxide was deposited by using the TEOS source in PECVD clusters. Gates, contacts, and interconnections were finally deposited and etched to have a good electrical connection between the designed TFTs. The IV characteristics are measured by using the HP4156B semiconductor analyzer.

3 THE CONVENTIONAL RPI MODEL

The RPI model is a SPICE compact TFTs model developed on the single crystalline MOSFET model [6]. This model contents following features:

1. Field effect mobility that becomes a function of gate bias
2. Effective mobility that accounts for trap states.
3. Reverse bias drain current function of electric field near drain and temperature.
4. A design independent of channel length.
5. A unified DC model that includes all four regimes for channel lengths down to 4 μm ; those four regions are: leakage (thermionic emission), subthreshold (diffusion-like model), above threshold (c-Si-like, with mFet), and Kink effect (impact ionization with feedback).
6. An AC model that accurately reproduces C_{gc} frequency dispersion.
7. An automatic scaling of model parameters that accurately model a wide range of device geometries

Though the vertical electrical field induced mobility degradation effect has been introduced in the RPI model, the expression could not reflect mobility behavior well. The mobility model used in RPI is represented as following function:

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_{U0}} + \frac{1}{T_{mul} \cdot \left(\frac{2 \cdot V_{gse}}{V_{sth}} \right)^{MMU}} \quad (1)$$

It is found from the n-channel TFT optimization result shown in Fig. 1 that one cannot model Gm characteristics well by using the conventional mobility model. In comparing with the measured data, when the measured Gm decreasing at the high gate bias region, the simulated Gm will sustain flat.

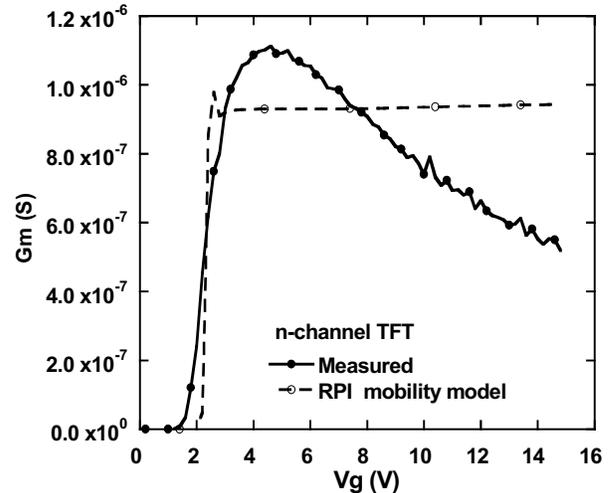


Figure 1: Comparison of the measured and simulated Gm characteristics for an n-channel TFT (width / length (W/L) = 20/4 [μm]).

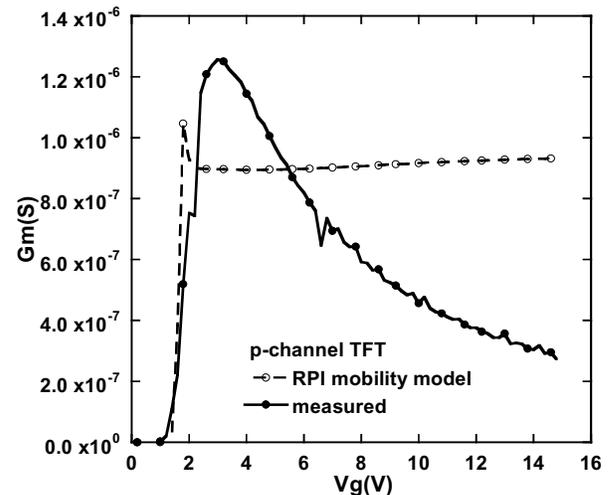


Figure 2: Comparison of the measured and modeled Gm characteristic for a p-channel TFT (width / length (W/L) = 20/4 [μm]).

Similar result is also found in the Fig. 2 that the p-channel TFT has a Gm decrement for the high gate bias condition; but the RPI model could not handle this characteristic well. The error of Gm should cause an

accumulation of inaccuracy and finally results a wrong circuit function. The problem will be more critical for analog circuit design.

4 THE PROPOSED MODEL

It is known that BISM 4 model is one of the most popular SPICE compact models for the simulation of deep sub-micron CMOS devices. The physical based mobility model is one of the most attractive features in the BISM 4 model. The model we considered here incorporates the following effects into the electron/hole mobility, they are: high field, substrate bias, and temperature effects. Owing to the fact that no body bias is usually applied on the TFT devices; therefore the substrate effects should not be considered. Accordingly, the proposed mobility model has the following form:

$$\frac{\mu_0}{1 + (U_a) \left(\frac{V_G + V_T}{T_{ox}} \right) + U_b \left(\frac{V_G + V_T}{T_{ox}} \right)^2} \quad (2)$$

Gm characteristics simulated with the modified mobility model are shown in the following two figures. It is found that the new mobility model greatly improves the high field Gm behavior for both the n-channel and p-channel TFTs. Those characteristics express the gate voltage reduced mobility effect successfully, owing to the better agreement of the Gm characteristics. It is expected that the simulation result of the TFT circuit will have higher correctness, especially for the AC simulations.

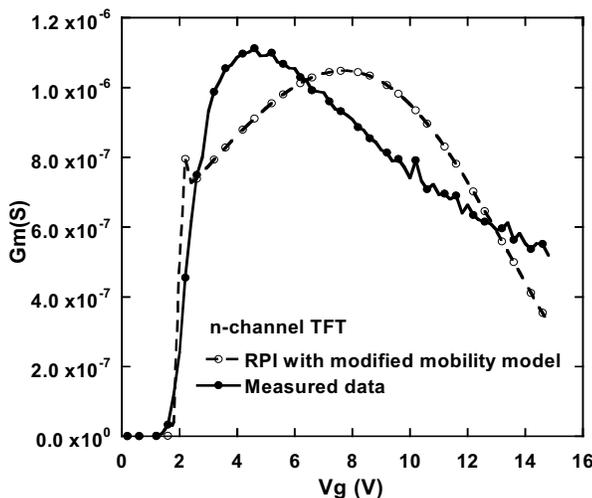


Figure 3: Comparison of the measurement and our new model for an n-channel TFT.

5 MODEL EXTRACTION

An auto-expiation tool that developed by our research team has been applied to perform the parameters extraction.

Tab. 1 shows the error calculated from measured data and RPI model. It should be noticed that RMS error at the high gate biased region would sustain above 3 percents, this is not acceptable for the most applications; however, could not make any improvement under the conventional mobility structure. The similar optimization process is also performed on our proposed mobility modified model. It could be found from Tab. 2 that our correctness will greatly enhance the agreement between the model and measured data. By using our mobility modification, the error can be easily reduced to less than 1 percent. In comparing with the conventional RPI TFT model result, the improvement is significant and easy to achieve.

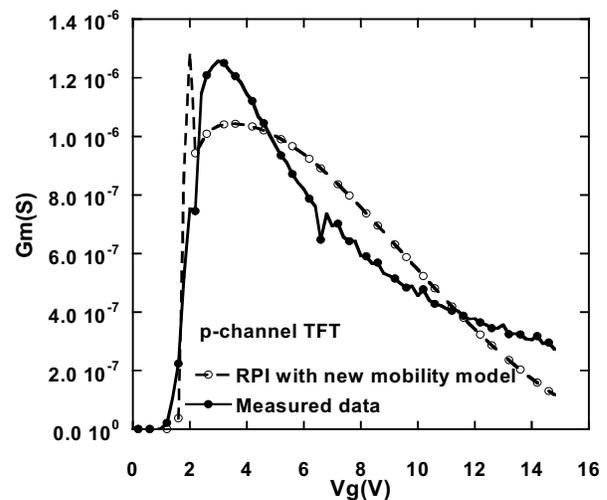


Figure 4: Comparison of the measurement and our new model for a p-channel TFT.

Table 1: Errors of the conventional RPI TFT model.

Measured Vth	2.0505 V
Extracted Vth	2.0500 V
RMS Error of I_D-V_D	3.73%
RMS Error of I_D-V_D in Sec.1	1.30%
RMS Error of I_D-V_D in Sec.2	3.19%
RMS Error of I_D-V_D in Sec.3	4.66%
RMS Error of I_D-V_G	3.33%
RMS Error of I_D-V_G in Sec.1	0.02%
RMS Error of I_D-V_G in Sec.2	1.35%
RMS Error of I_D-V_G in Sec.3	7.01%

Table 2: Errors of the proposed model.

Measured Vth	2.0505 V
Extracted Vth	2.0381 V
RMS Error of I_D-V_D	0.94%
RMS Error of I_D-V_D in Sec.1	0.45%
RMS Error of I_D-V_D in Sec.2	0.48%
RMS Error of I_D-V_D in Sec.3	1.32%
RMS Error of I_D-V_G	0.60%
RMS Error of I_D-V_G in Sec.1	0.01%
RMS Error of I_D-V_G in Sec.2	0.65%
RMS Error of I_D-V_G in Sec.3	1.11%

6 IV CHARACTERISTICS SIMULATION

Output characteristics have been simulated in this work and shown in the following two figures. It is found that the high field mobility effects dominate output characteristics at high gate biased situations. This point is the most important way when designing the driving circuit by using the complementary TFT devices. This is causing from the fact that driving capability will be strongly affected by the output resistance. Therefore, a precisely modeling of high field mobility is not only helpful in device fabrication but also essential in TFT circuit design. Observing from the modeling results, a better agreement will be found, especially for the p-channel TFT. Those superior characteristics are mainly based on the correctness of the proposed mobility model.

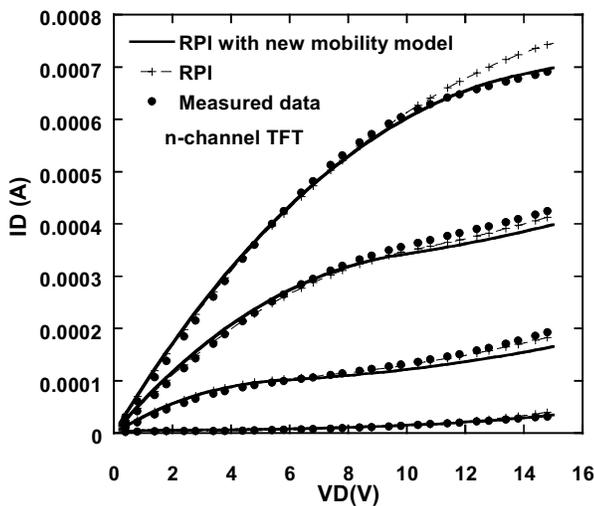


Figure 5: Comparison of the measured n-channel TFT output characteristics between the RPT, and new mobility models.

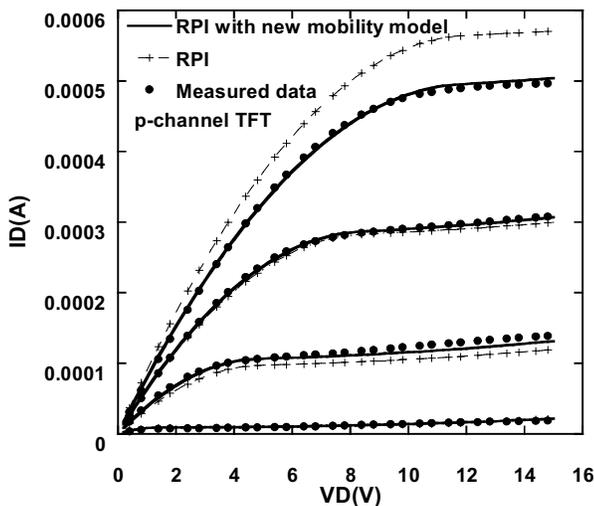


Figure 6: Comparison of the measured p-channel TFT output characteristics between the RPT, and new mobility models.

7 CONCLUSIONS

It has been demonstrated that the mobility modified RPI model will greatly improve the agreement between the experimental device and models. With the modification, the optimization process could be easily achieved; moreover, no additional complexity is added. The convergence and efficiency tests have been also done on the SPICE circuit simulator, it is proven that no convergence and efficiency problems are found.

To verify the usability of the new model, the convergence test should be done on SPICE circuit Simulator. After a series tests, it has been found that no any convergence problem existed in our model. Computationally it has shown very good efficiency in different testing cases.

8 ACKNOWLEDGEMENTS

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