Adaption of the 3ω-Method for Testing of MEMS

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ABSTRACT

The 3ω-method was introduced several years ago to measure the thermal conductivity of bulk materials. Since then various modifications have been reported, which have increased the range of applications significantly. As a purely electrical method, it is appropriate for automated wafer level testing. However some extensions have to be implemented to meet the special requirements of wafer level testing. We present an implementation for coating layers and we show how these layers can be used to simulate the surrounding air when no vacuum conditions are available.

Keywords: thermal conductivity, 3ω-method, testing

1 INTRODUCTION

Automated wafer level testing of MEMS requires methods to measure geometry and material related parameters by purely electrical means [1]. The 3ω-method [2], [3] to measure the thermal conductivity seems to be appropriate for this task. A periodic heating current at angular frequency ω is applied to a temperature dependent resistor (Fig. 1), producing Joule heating at frequency 2ω. Amplitude and phase of the resulting thermal wave depend on the geometrical and thermal parameters of the device under test. Due to the nonzero temperature coefficient of the heater there is a small oscillation of the resistance at frequency 2ω, leading to a tiny 3ω-component in the voltage. This 3ω-voltage is measured with lock-in techniques and the amplitude of the temperature oscillations can be calculated by [3]

$$\Delta T = 2\frac{dT}{dR}R\frac{U_{3\omega}}{U_{1\omega}}. \qquad (1)$$

The 3ω-method is purely electrical, non-destructive and compatible with typical MEMS processes. Furthermore, it permits the determination of multiple parameters: while the original 3ω-method as presented by Cahill et al. [3] is capable of measuring the thermal conductivity and thermal capacity of bulk materials, modifications of this method can be used to measure also the thermal conductivity of a thin film on a substrate (offset-method) [4] or anisotropic thermal conductivity (with heaters of different widths) [5]. However, these methods make high demands on the device under test, that are generally not fulfilled by typical MEMS. The offset-method, for example, requires a (thermally) thin film with low thermal conductivity on a (thermally) thick substrate with high thermal conductivity to ensure quasi one-dimensional heat transport through the thin film.

Recently, Kim et al. [6] and Borca-Tasciuc et al. [7] have proposed mathematical models for the 3ω-method on multilayer systems, considering finite substrate thickness, anisotropic thermal conductivity, thermal boundary resistances and finite heater capacitance. The range of samples that the 3ω-method can handle is drastically increased by fitting experimental temperature oscillations with these models.

We have modified the models to include also coating layers on top of the heater. Our modified model is outlined briefly in section 2. Experimental results are presented in section 3, where we first demonstrate the excellency of our fits for a well-known two layer system. Then we show the effect that results from a coating layer on a 100μm porous silicon cavern etched in a silicon substrate. Finally, we show that surrounding air can be treated as such a coating layer. This is essential for automated wafer level testing since these measurements are commonly performed at ambient pressure. Experimental data in vacuum and in air are provided.

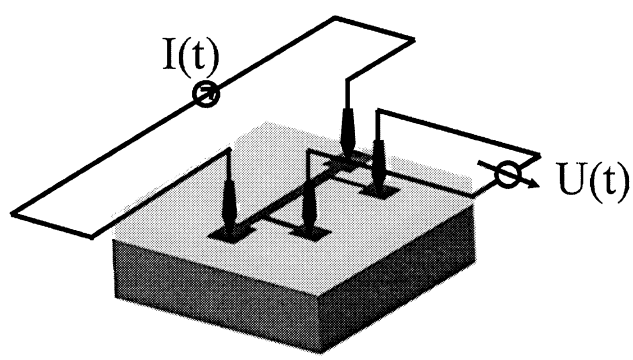

Figure 1: Experimental setup for the 3ω-method on a thin film on substrate system. The heater is deposited on the multilayer system by standard thin film technology.

2 HEAT FLOW IN MULTILAYERS

We consider a multilayer system where layer 1 is the topmost layer while layer N is the substrate. The heater is at interface j between the layers $n = j$ and $n = j + 1$. Heat is produced at the angular frequency 2ω, the heating power is P, while b and l are the heater half width and length, respectively. Neglecting the heater thickness and heat capacity, the temperature oscillations of the heater can be calculated as

$$\Delta T = \frac{P}{2\pi l b^2} \int_0^\infty f(m) \frac{\sin^2(mb)}{\gamma_1 m^2} \, \mathrm{d}m, \qquad (2)$$

where

$$f(m) = \frac{(B^+(m) + B^-(m))(A^+(m) + A^-(m))}{A^+(m)B^-(m) - A^-(m)B^+(m)} \qquad (3)$$

and

$$\gamma_n = \kappa_n \sqrt{\kappa_{n,xy} m^2 - i\frac{2\omega}{D_n}}. \qquad (4)$$

κ_n is the cross-plane thermal conductivity of layer n, $\kappa_{n,xy}$ is the quotient of cross-plane and in-plane thermal conductivity of layer n. D_n is the thermal diffusivity of layer n. The parameters A^+, A^-, B^+ and B^- are calculated by a matrix procedure given by Feldman [8]. Although the procedure given by Feldman is one-dimensional, it can be applied to two-dimensional heat flow by Fourier transforming the diffusion equation.

The finite heat capacity and thickness of the heater as well as an interfacial thermal resistance can be taken into account by a simple network model [7]

$$\Delta T^* = \frac{\Delta T + R_{\mathrm{th}} P/(2bl)}{1 - 2\mathrm{i}\omega c_h d_h (R_{\mathrm{th}} + 2bl\Delta T/P)}. \qquad (5)$$

Here, ΔT is the result of Eq. 2, c_h is the heat capacity per unit volume of the heater, d_h is the heater thickness and R_{th} is the interfacial thermal resistance between the heater and the adjoining layer(s).

3 EXPERIMENTAL RESULTS

In section 3.1 we demonstrate the ability of the 3ω-method on the well-known system of a Si substrate with a SiO_2 layer. In section 3.2 we present measurements on a porous silicon cavern with a SiO_2 coating layer and show the influence of this coating layer on the 3ω-signal. Finally we measure the porous silicon samples also at ambient pressure and show, that the surrounding air can be treated as an additional layer with thermal conductivity $\kappa_{\mathrm{air}} = 0.045\mathrm{W\ m^{-1}K^{-1}}$.

3.1 TWO LAYER SYSTEM

Figure 2 (a) shows schematically the silicon substrate with a PECVD SiO_2 layer and a Pt heater. The thicknesses of the oxide layers for two samples has been measured with white light interferometry to be $d_{opt} = 2113$nm and $d_{opt} = 1018$nm, respectively. The heater width is $2b = 14.4\mu$m. Figure 3 shows the measured temperature oscillations for the two systems together with calculations according to Eq. 5[9]. The finite thermal conductivity of the heater is not taken into account, but one can estimate the maximum influence to be less then 10^{-3}K by treating the heater as an additional layer.

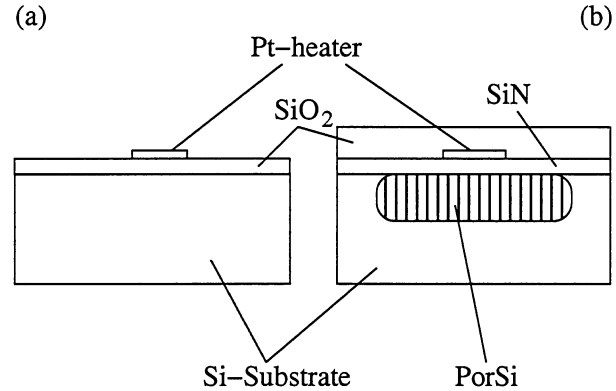

Figure 2: Schematical cross section of the samples (not true to scale). The sample (a) consists of a 500μm Si substrate with a 2μm respectively 1μm SiO_2 film and a 150nm Pt heater. For sample (b) a 100μm porous silicon cavern has been etched in the Si substrate. The 150nm Pt heater is on a 100nm SiN layer, covered by 400nm SiO_2.

We have shown that the four physical parameters thermal conductivity κ_1 and thickness d_1 of the layer, the thermal conductivity of the substrate κ_2 and the heat capacity of the heater c_h can be determined by a single measurement over the frequency range 10Hz – 200kHz [9]. With the commonly used frequency range 10Hz – 10kHz it is only possible to determine κ_1 when d_1 is known from additional (non-electrical) measurements.

Table 1 shows the results of the fitted parameters. The thermal condutivities and the capacity of the heater are in good agreement with literature values ([10]–[13]).

Table 1: Results of the four-parameter fit for two SiO_2 thicknesses. The optically measured film thickness is also given.

d_{opt} nm	d_1 nm	κ_1 W/(mK)	κ_2 W/(mK)	c_h MJ/(m^{3}K)
2113	2248	1.10	143	2.4
1018	1167	1.15	146	2.2

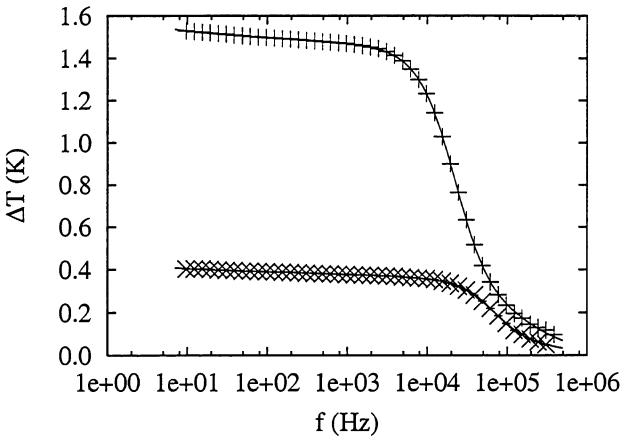

Figure 3: Measured (symbols) and calculated (full lines) temperature oscillations for a 2μm (+) and a 1μm ($\times$) SiO_2 layer on a Si substrate using best fit parameters κ_1, d_1, κ_2 and c_h.

3.2 MULTILAYER SYSTEM

Our multilayer system consists of a 100μm porous silicon cavern, etched in a Si substrate (Fig. 2 (b)). The cavern is covered with a 100nm SiN layer. On top of the SiN layer is the 150nm thick Pt heater and a 400nm coating PECVD SiO_2 layer.

Figure 4 shows the measured temperature oscillations versus the frequency and the calculation considering (full drawn line) and neglecting (dashed line) the coating SiO_2 layer. For the porous silicon $\kappa_{xy} = 0.45$ and $\kappa = 0.89$W m^{-1}K^{-1} have been used. This is in good agreement with literature values on similar samples [14]–[16].

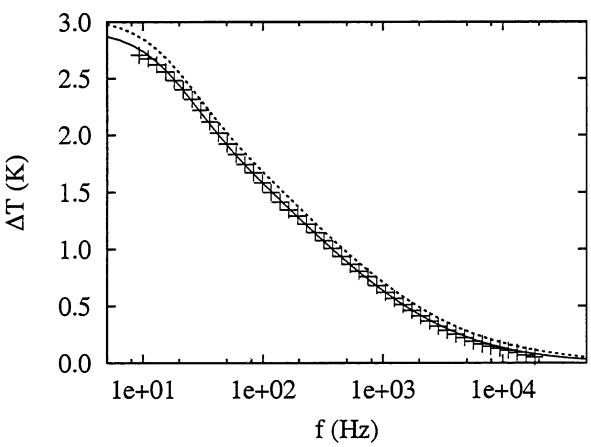

Figure 4: Measurement on a 100μm porous silicon cavern (symbols). The dashed line is calculated neglecting the 400nm coating SiO_2, while this layer is considered for the calculation of the full drawn line.

The measurements of Fig. 4 were carried out in a vacuum chamber at 10^{-2}mbar in order to eliminate heat conduction through the surrounding air. We have investigated this effect by performing a reference measurement at ambient pressure. The result is shown in Fig. 5 (a) (in-phase-component of the temperature oscillations) and (b) (out-of-phase-component). This measurement was analysed by simulating the air as a semi-infinite layer on top of the PECVD SiO_2 layer. The thermal condutivity and thermal capacity of the air layer were used as fit parameters, yielding the result $\kappa = 0.045$W m^{-1}K^{-1} and $c = 2.2$ kJ m^{-3}K^{-1}. These values are larger than the literature values for dry air ($\kappa_{\text{lit}} = 0.025$W m^{-1}K^{-1} and $c_{\text{lit}} \approx 1.2$ kJ m^{-3}K^{-1} [17], [18]). However the literature values relate to pure conduction, neglecting convective effects while we measure the combined effect of conduction and convection.

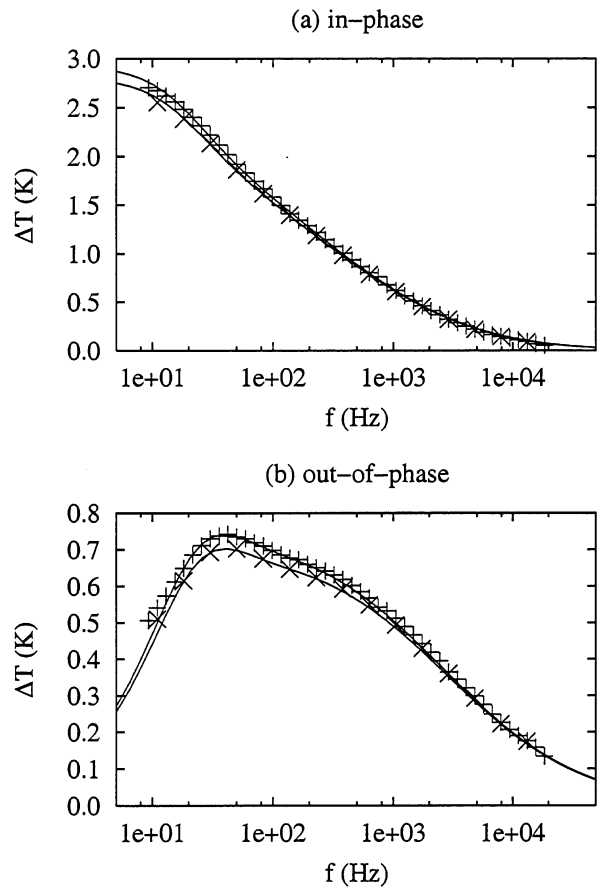

Figure 5: The influence of the surrounding air on 3ω-measurements ($\times$). The measurement at 10^{-2}mbar of Fig. 4 is plotted as reference (+).

Vacuum conditions are normally not available for automated wafer level testing. However the excellent agreement of measurement and calculation in Fig. 5 suggest the possiblity of correcting the influence of the air.

4 CONCLUSION

The range of samples that can be measured with the 3ω-method has been drastically increased in the last years. In this article we have presented a modification of the up-to-date models to handle also multilayer systems with coating layers on the heater. We have shown experimentally that surrounding air can be treated as such a coating layer. This makes the 3ω-method ideally suited for automated wafer level testing of MEMS, where normally no vacuum conditions are available. Another possible application in this context is the testing of the encapsulated pressure in vacuum sealed MEMS packages such as acceleration or angular rate sensors.

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