Starting Over: g_m/I_d-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies

Daniel Foty[1], David Binkley[2], and Matthias Bucher[3]

Abstract – **A method of interpreting MOSFET behavior is described which is more coherent for modern analog CMOS circuit design. This method supercedes the use of simple but antiquated equations in design, and replaces them with an approach based on the inversion coefficient of the individual transistors in the design. Measurements and modeling confirm that this method can be used directly to arbitrate among the various countervailing requirements of demanding analog designs.**

1 Introduction

As technology has advanced, the behavior of the simple MOSFET has become more complicated, due to smaller geometries, higher electric fields, and (more recently) a continuing decrease in the power supply voltage [1]. Despite these changes, analog design approaches have basically continued to use methods based on much older and simpler interpretations of MOSFET behavior. This has led to an analog "design gap," in which designers are trying to make old methods work on new technology; this is preventing designers from realizing the full potential of modern deep submicron CMOS technology.

In this paper, we will present a more modern method of evaluating and characterizing MOS technology for analog design. Based on the concept of MOS inversion coefficient (IC), this method provides a designer with straightforward access to key design figures-of-merit, such as small-signal parameters. This in turns permits a coherent path to evaluating design trade-offs without resorting to either flawed hand calculations or time-consuming "trial-and-error" circuit simulations.

2 Hand Calculations for Analog Design

Approaches to analog design usually involve hand calculations; these hand calculations involve interpretations of MOSFET behavior which were once valid, but which largely fail for modern CMOS technology. As a result, hand calculation ability is limited to some special cases; for example, in large MOSFETs, the old "square-law" is relatively valid for transistors operating in strong inversion and saturation, while a simple exponential I-V description works well in weak inversion. In the extreme short-channel limit, the "square-law" becomes linear and also loses its 1/L dependence.

Aside from these cases, no good hand calculation methods are available for the MOSFET. A perusal of various analog design texts shows that this problem is overcome largely by ignoring it – design and analysis are carried out under the assumption that the "square-law" is valid. Use of these assumptions has tended to not be fatal, since they actually err on the side of caution; for example, if the "square-law" is used to compute the saturation voltage for transistor biasing, it will be considerably overpredicted. This is not a problem when the supply voltage is relatively large (e.g. 5V), since there is considerable margin for error. However, in modern processes (e.g., at the 0.13μm technology node, $V_{dd} = 1.2V$), there is little margin for such error. For example, in a simple cascode with two transistors and a load, the "voltage budget" across these three elements is very tight and cannot afford any waste based on an antiquated calculation of V_{dsat}.

A further problem with transistor biasing flows from the tight voltage budget. Designers are forced to use lower DC gate voltages to keep transistors biased in saturation; this forces transistors to be biased in moderate inversion (rather than strong inversion), a region where there are no reasonable hand calculation approaches. Designers are often unaware of the bias levels of the transistors in the designs. Clearly, a more modern and coherent approach is required.

3 Normalization Using Level of Inversion

A more sensible approach to interpreting the MOSFET for analog design can be based on the level

---

[1] Gilgamesh Associates, Fletcher, Vermont, USA; dfoty@sover.net.
[2] University of North Carolina/Charlotte, Charlotte, North Carolina, USA; dmbinkle@uncc.edu.
[3] National Technological University of Athens, Zagraphou, Athens, Greece; mbucher@elab.ntua.gr.

of inversion (or inversion coefficient, IC) [2]; this concept was originally elucidated by Vittoz [3] and others. This method provides a useful way of identifying the operating region and inversion level of MOS transistors; if the level of inversion can be identified, it can then be used as a design variable for circuit optimization. This represents a very different way of thinking when compared with "conventional" analog design methods, in which the transistor bias current is the main item used in design and analysis.

The inversion coefficient [3] is defined as

$$IC = \frac{I_D}{2n\mu_0 C_{OX}(W/L)U_T^2} = \frac{I_D}{2nk_0(W/L)U_T^2} , \quad (1)$$

where I_D is the drain current, n is the slope factor, μ_0 is the low-field mobility, C_{OX} is the gate oxide capacitance, U_T is the thermal voltage (kT/q), $k_0 = \mu_0 C_{OX}$, and W and L are the effective channel width and length respectively. Although n has slight gate bias dependence (decreasing with increasing gate bias), it is assumed constant here. The inversion coefficient can be expressed in simplified form as

$$IC = \frac{I_D}{I_0(W/L)} , \quad (2)$$

where I_0 is a process dependent current equal to $2nk_0U_T^2$; that is, I_0 is the drain current of a unity shape factor device ($W/L = 1$) at the center of moderate inversion where $IC = 1$.

The best method of interpreting the inversion coefficient is via the efficiency of the transconductance (the transconductance-to-current ratio), g_m/I_D; g_m/I_D is fundamental to the MOSFET, and also provides a direct guide to the gain of FET-based operational amplifiers. By evaluating g_m/I_D against I_d (rather than against V_g), a surprising amount of insight can be gained into MOSFET operation. In fact, this interpretation can serve to define *all* of the key elements of MOSFET behavior of interest to the analog designer.

4 Measurements

As an example, measurements were made on a 0.5μm CMOS technology using a custom semiconductor parameter analyzer. The analyzer has a 10-decade drain current range covering 10 pA to 100 mA, with most measurements made over a 1 nA to 10 mA range (7 decades) at an accuracy of approximately 0.1%. A/D and D/A conversion resolution is 16 bits.

Figures 1 and 2 contain measured results for (respectively) nMOS and pMOS devices over more than 7 decades of inversion level ($IC < 0.001$ to $IC > 1000$). The asymptotes of ideal transconductance efficiency in weak and strong inversion (neglecting short-channel effects) are indicated. The roll-off of transconductance efficiency is clearly observed for inversion levels above weak inversion; the transconductance efficiency is nearly identical for the 0.5μm to 33.4μm range of channel lengths. At high levels of strong inversion, an additional degradation with respect to the ideal asymptotes occurs for short-channel devices due to short-channel effects.

Measurements in the form of Figures 1 and 2 provide *fundamental* information to the designer regarding the MOS technology which has been characterized in this way, as will be discussed below.

5 Modeling

As noted earlier, the transconductance-to-current ratio g_m/I_D is fundamental to the MOSFET. However, despite its importance, this ratio has received very little attention in the development of MOSFET models which are used in circuit simulations. Virtually all popular MOS models fail (both structurally and parametrically) to properly model g_m/I_D over the range of weak, moderate, and strong inversion.

The one presently-available exception is the EKV MOSFET model [4]. This model was developed with a clear focus on *analog design usage*, and thus includes the modeling of g_m/I_D as fundamental to the model structure. Proper modeling of the measured behavior is required if this fundamental MOSFET behavior is to be translated into direct analysis and circuit simulations.

Figures 1 and 2 show model results obtained with an EKV v2.6 MOS model [4] parameter set extracted for this process. (A single parameter set is used for all geometries.) The model shows proper qualitative behavior over the range of inversion levels, with particularly accurate results in weak and moderate inversion. In very strong inversion, the model remains accurate for long-channel devices, while the transconductance efficiency is slightly overestimated for the shorter-channel devices; these samples exhibited considerable self-heating in the short-channel devices, which likely is the main contributor to these minor discrepancies.

6 Design Interpretation

Given the earlier discussion of obsolescent analog design practices, some implications of this work can now be considered in that context.

In typical practice, analog designers begin by arbitrarily selecting the bias current for transistors in a design. From those currents and the information on the process technology which is available, transistor widths are selected. Design iteration then commences, as the designer adjusts currents and device dimensions to meet the specific design goals.

Just in that form, there is clearly inherent danger. If items such as bias current and channel width are treated as "knobs," the inevitable result will be a not-very-well-controlled design process in which adjustments and rechecking can go on almost indefinitely.

This situation was bad enough in the days when both voltage bias levels and design goals were rather relaxed by present-day standards. However, with both decreasing V_{dd} and more demanding design goals (in terms of lower power consumption, more signal processing sensitivity, etc.), the available margin for error is considerably smaller. Confronted with this situation and a larger number of "knobs," analog designers can rapidly find themselves churning in circles, making adjustments while hoping that the design process will eventually head in the right direction.

As noted earlier, a prominent example is the tight "voltage budget" in cascode circuits. A designer can start with a bias current and find a channel width and gate voltage biases which keep the transistors in saturation; however, this approach contains no information about the inversion level of those transistors!

The approach described here allows the inversion level of the transistors to be made *fundamental to the design process*, rather than being an accident of the particular bias currents and transistor sizes which occur in a design. Knowledge of the inversion level allows for a proper evaluation of the design trade-offs among gain, bandwidth, transistor size, matching, etc. [5]. If a designer optimizes the transistors based on inversion level, then channel width follows as a *consequence* of the design (rather than as an input).

As is well-known (and abundantly clear from Figures 1 and 2), weak inversion favors DC gain, while strong inversion favors bandwidth. Within the context of these trade-offs, moderate inversion has emerged as a region which offers an optimized compromise amongst the numerous constraints. By evaluating the MOSFET in the fashion described here, circuit designs can be optimized in a fashion which is both *coherent* and *timely*.

7 Conclusions

As noted at the outset, the objective of this paper was not merely to present a tool-box method for analog design; more grandly, the goal was to inspire a more overarching rethinking and reinterpretation of the MOSFET in the context of modern technology and modern analog design practices.

Except for special cases, there are no simple hand-calculation methods for evaluating MOSFET behavior in an analog circuit design. While the use of such hand calculation approaches has been obsolete for some time, more recent constraints have caused those methods to literally become dangerous. Clearly, a more realistic method of describing MOSFET behavior is required. In terms of modern analog design, the most sensible course is to use the inversion level of the circuit's transistors as the foundation.

By *interpreting* MOSFET behavior in the fashion described here, and then employing *MOS modeling techniques* which are consonant with that fundamental behavior, the door is opened to new and more coherent approaches to analog design in modern deep submicron CMOS processes.

References

[1] D. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall, 1997.

[2] D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS over the Continuum of Inversion Level and Channel Length," *Proceedings of the 7th IEEE International Conference on Electronics, Circuits, and Systems (ICECS2000)*, pp. 161 – 164.

[3] E. Vittoz, "Micropower Techniques," in *Design of MOS VLSI Circuits for Telecommunications* (ed. J. Franca and Y. Tsividis), Prentice-Hall, 1994.

[4] M. Bucher et al., "The EPFL-EKV MOSFET Model Equations for Simulation, Version 2.6," Technical Report, EPFL, June 1997.

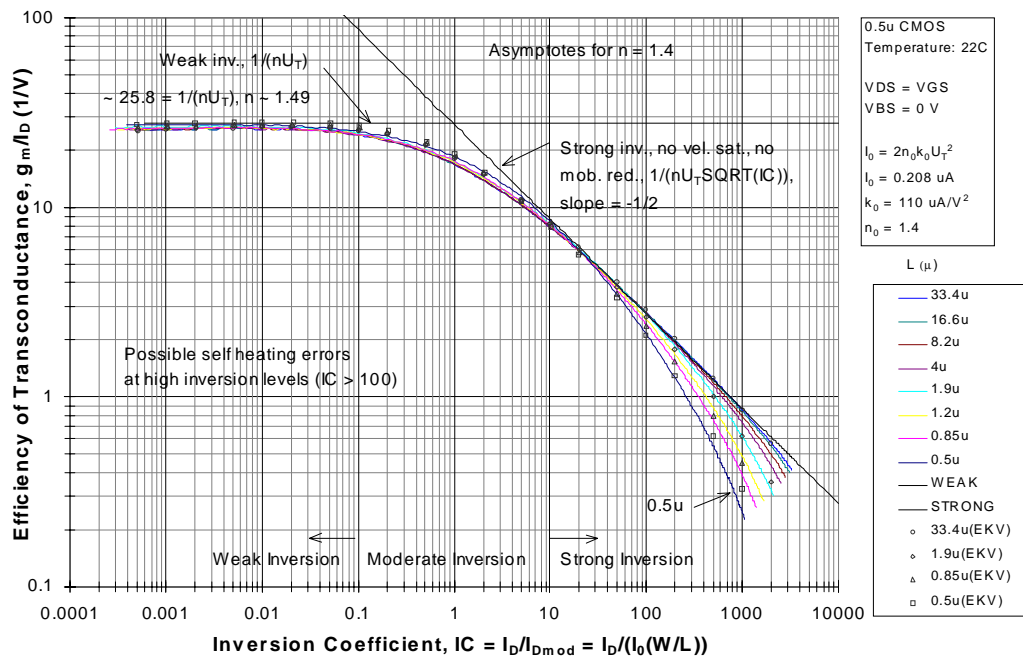[5] D. Binkley, M. Bucher, and D. Foty, text in preparation.

Figure 1. nMOS g_m/I_D vs. inversion coefficient from weak through strong inversion for L = 0.5μm - 33.4μm; measurement (lines) and EKV v2.6 MOS model (markers).
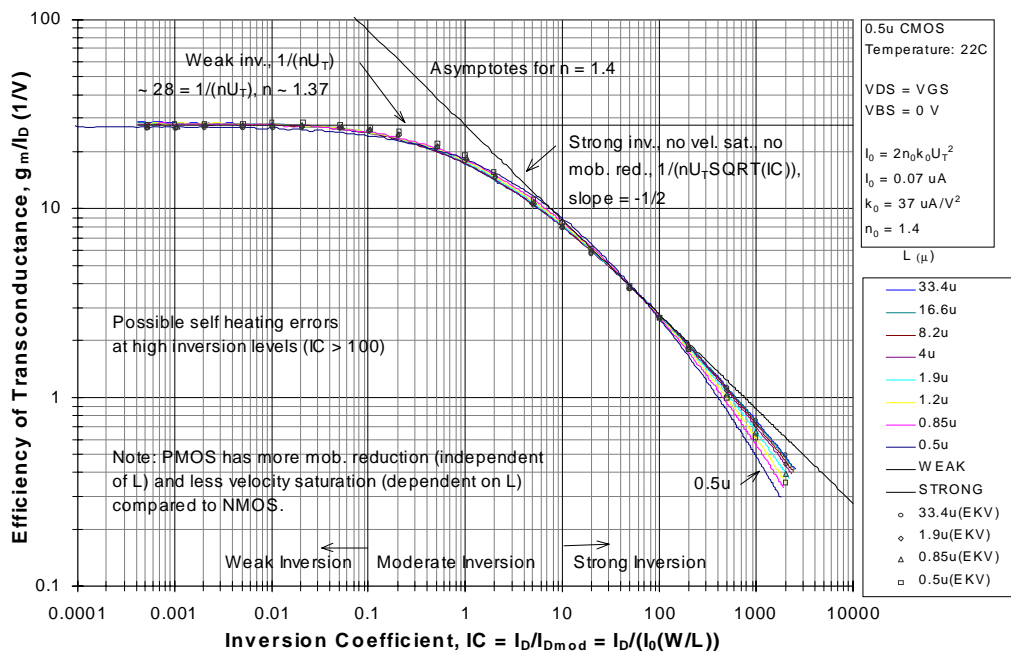

Figure 2. pMOS g_m/I_D vs. inversion coefficient from weak through strong inversion for L = 0.5μm - 33.4μm; measurement (lines) and EKV v2.6 MOS model (markers).