

# Hot-Carrier-Induced Current Degradation in Deep Sub-Micron MOSFETs from Subthreshold to Strong Inversion Region

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## ABSTRACT

Reliability is an important requirement for almost all users of integrated circuits. It becomes more challenging in advance technologies as devices are scalding down. In this paper, we study the device performance degradation caused by hot-carrier stress in advance technologies. The device performance degradation is caused by the interface traps generated under hot-carrier stress. The interface traps induce the device performance degradation by affecting the mobility and surface potential. As it is correlated to the drain and gate voltage conditions, the degradation behavior will vary from linear to saturation region and from weak inversion to strong inversion region. It is verified with numerical simulations and experimental data.

**Keywords:** Reliability, MOSFET, substrate current, interface states, performance degradation, transconductance, device lifetime.

## 1 INTRODUCTION

In the past decades, as predicted by the Moore's law, the IC circuit density increases to reduce the cost per chip and to achieve better performance. With critical device dimensions scaling down, the electric field increases due to device dimension scaling being much more aggressive than operation voltage scaling, and reliability problems are becoming more and more important especially in recent years while the MOSFETs enter the nanoscale era. The three major mechanisms in device performance degradation are hot-carrier induced degradation, negative bias temperature instability (NBTI), and positive bias temperature instability (PBTI). NBTI is based on traps for holes and it is an important concern in p-channel devices. PBTI starts to play an important role with the introduction of the high-k materials. It is based on electron trapping, and therefore, it is important in n-channel devices. In n-channel devices, hot-carrier induced degradation is another important reliability concern. With high electric fields, some electrons are accelerated to attain a very high kinetic energy, which can be injected into the gate dielectric layer. These electrons that are injected into the gate dielectric will be trapped by trap centers located in the gate dielectric or cause to generate the interface states. There are four

injection mechanisms for hot carriers injection into gate dielectric: channel hot-electron (CHE) injection, drain avalanche hot-carrier (DAHC) injection, secondary generated hot-electron (SGHE) injection, and substrate hot-electron (SHE) injection [1-5]. CHE injection is the dominant one in HCI degradation and it can be monitored by gate current or substrate current, in this study the substrate current is used since it is easier to be measured than gate current in deep-submicron devices and as gate oxide scaling down the direct tunneling current becomes significant in gate current; therefore, the gate current caused by trapping and de-trapping becomes less significant in total gate current. For n-channel MOSFETs (NMOS), the degradation caused by HCI is more severe than degradation caused by NBTI and PBTI. In this work, we only study the performance degradation caused by HCI in NMOS.

## 2 ANALYSIS OF HCI DEVICE PERFORMANCE DEGRADATION

The physical mechanisms for HCI have been extensively studied [6-8], under high channel electric field the hot carriers injected into the oxide induce the generation of interface traps, and the interface trap results in the current and transconductance degradation since interface traps will affect the surface potential and mobile carriers mobility. Figure 1 shows the linear region current and transconductance degradation after hot carrier stress, the open symbols are fresh device and the filled symbols are degraded device after 500 minutes hot carrier stress. Two devices with different oxide thickness are shown. After 500 minutes hot carrier stress,  $I_{din}$  degraded to 96% and 97% in thick oxide (stress condition:  $V_{ds}=V_{gs}=2.75V$ ) and thin oxide (stress condition:  $V_{ds}=V_{gs}=1.4V$ ) devices, respectively. Under the same stress condition, more severe performance degradation occurred in devices with thinner gate oxide.

In IC design, accurate predict of the circuit life time requires accurate simulation of device performance degradation. Device life time, performance degradation rate, and device age are some important concepts to characterize device reliability. Device life time is defined as the time at which the device performance degradation reaches a criterion under certain operating condition. The criterion can be  $-10\% I_{dsat}$  or  $100mV \Delta Vt$ , and so on. The

degradation is defined as a function of  $At$ , where  $A$  is the device performance degradation rate,  $t$  is the applied stress time, and  $At$  is defined as device age. Device age can be used to quantify the amount of device degradation. In NMOS devices, the HCI degradation is approximated by  $\Delta D=(At)^n$  where  $n$  is about 0.3 for the reaction limit rate. The expression for the average interface trap density caused by hot carrier stress is given as some function of substrate current,  $I_{sub}$  [6]:

$$N_{it} = C \left( T_{Stress} \left( \frac{I_{sub}^3}{I_{Drain}^2 W} \right) \right)^n, \quad (1)$$

where  $C$  is a technology dependent constant,  $T_{Stress}$  is the stress time, and  $n$  is a fitting parameter. And a model predicting device lifetime,  $\tau$ , which is proportional to  $(I_{sub}/I_{ds})^{-3}/I_{ds}$  is developed by Hu. Therefore, an accurate simulation of the  $I_{sub}$  is necessary for accurate device degradation simulation. In this work, the  $I_{sub}$  is expressed as: [6]

$$I_{sub} = \frac{A_i}{B_i} (V_{ds} - V_{dsat}) I_{ds} \exp\left(\frac{B_i l_c}{V_{ds} - V_{dsat}}\right), \quad (2)$$

where  $A_i$ ,  $B_i$ ,  $l_c$  are fitting parameters and  $V_{dsat}$  is the drain-source saturation voltage. Figure 2 shows the comparison between the measurement data and model of  $I_{sub}$  using Equation (1). With  $L = 280$ -nm NMOSFET,  $I_{sub}$  is shown in Figure 2(a) with different  $V_{ds}$ ,  $I_{sub}$  increases first and the largest  $I_{sub}$  occurs at around  $V_{gs}=0.5V_{ds}$ , after that it will decrease. Larger  $I_{sub}$  caused by higher  $V_{ds}$  is also shown. However, Figure 2(b) shows that the highest  $I_{sub}$  does not occur around  $V_{gs}=0.5V_{ds}$  in deep sub-micron device ( $L = 50$ nm,  $60$ nm, and  $80$ nm). In long channel devices, the  $I_{sub}$  curve is shown as a well-known bell-shape curve, we can observe that  $I_{sub}$  has a maximum point with respect to gate voltage at  $V_{gs}=0.5V_{ds}$ . Increase in  $V_{gs}$  will lead to an increase in drain current,  $I_d$ ; therefore,  $I_{sub}$  will also increase. However, while  $V_{gs}$  continue increasing,  $I_{sub}$  will start to decrease due to drain-source saturation voltage also increasing, and increase in  $V_{dsat}$  leads to a decrease in the channel electric field; therefore,  $I_{sub}$  will increase to some peak value and then start to decrease. Different from long channel devices, in short channel devices, due to velocity saturation/overshoot and the strong halo implant effect the channel electric field is not affected significantly by increasing  $V_{gs}$ . Therefore, substrate current does not reach the maximum point around the gate voltage at  $V_{gs}=0.5V_{ds}$ . In short channel devices, it will continue increasing at increasing gate voltage.

In NMOS, the device performance degradation is caused mostly by the electron interface trap, which is defined as an electrically neutral trapping potential well that can bind only one electron. The charge formulae of neutral electron traps  $Q_{ETi}$  is given by [9]

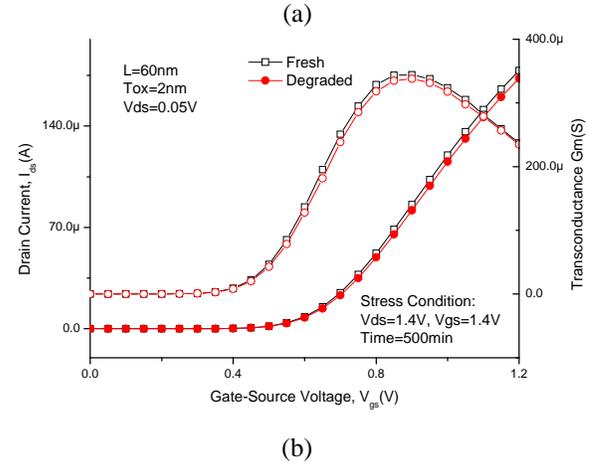
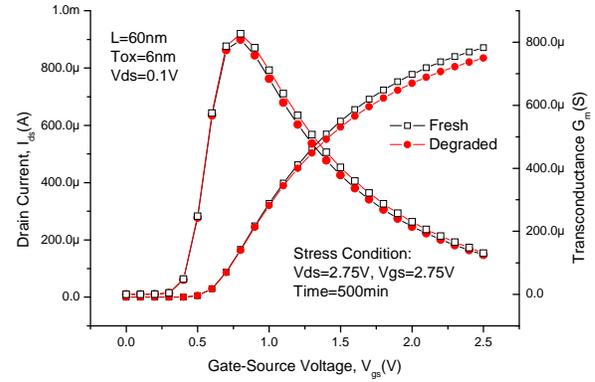
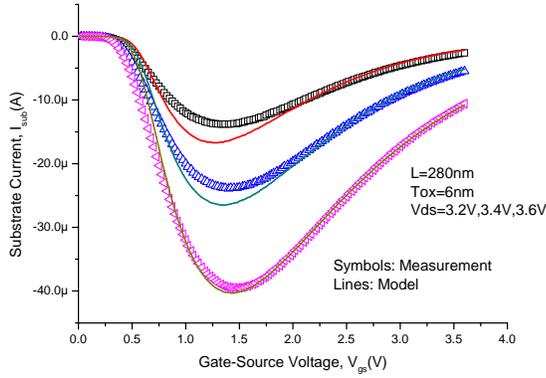


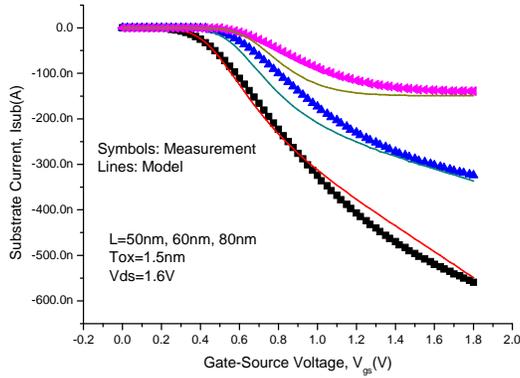
Figure 1: Fresh and degraded I-V and transconductance characteristics of NMOSFET as a function of  $V_{gs}$  (1)  $T_{ox}=6$ nm (2)  $T_{ox}=1.5$ nm.

$$\begin{aligned} Q_{it} &\approx Q_{ETi} = -qN_{ETi} \times F_{ETi} \\ &= -qN_{ETi} \times \frac{c_{ns}n_s + e_{ps}}{c_{ns}n_s + e_{ns} + c_{ps}p_s + e_{ps}}, \end{aligned} \quad (3)$$

where  $Q_{it}$  is total charge formulae of interface traps,  $N_{ETi}$  is the neutral electron-trap density ( $\text{cm}^2\text{eV}$ ) at the  $i$ th energy level.  $c_{ns}$  and  $c_{ps}$  are the electron and hole capture-rate coefficients,  $e_{ns}$  and  $e_{ps}$  are the electron and hole emission-rate coefficients, and  $n_s$  and  $p_s$  are the electron and hole surface concentrations. As anticipated by Equation (3), the charge trapping rate is closely related to the surface carrier concentration which is a function of the surface potential, and hence, the applied gate voltage. Thus, interface-trap charge is determined not only by interface-trap density but also by the charge trapping rate. Equation (3) can be solved together with Poisson's equation and the numerical result is shown in Fig. 3, for a device with large interface-trap densities, the interface-trap charge is small near the intrinsic region because of the low charge trapping rate while it is large in strong accumulation and inversion ranges because nearly all the interface traps are trapped with a hole or an electron.



(a)



(b)

Figure 2: Substrate current versus  $V_{gs}$  of NMOSFET (1)  $T_{ox}=6\text{nm}$ ,  $L=280\text{nm}$  with different  $V_{ds}$ , (2)  $T_{ox}=1.5\text{nm}$ ,  $V_{ds}=1.6\text{V}$ , and  $L=50\text{nm}$ ,  $60\text{nm}$ ,  $80\text{nm}$ .

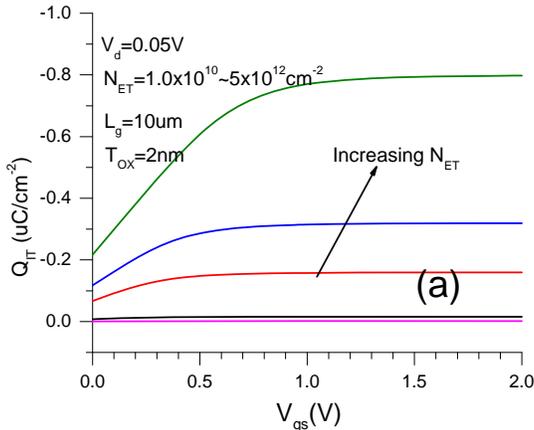


Figure 3. Gate-voltage dependence of interface-trap charges at various neutral electron interface-trap densities  $N_{ET} = N_{HT} = 1.0 \times 10^{10}$ ,  $1.0 \times 10^{11}$ ,  $1.0 \times 10^{12}$ ,  $2.0 \times 10^{12}$ , and  $5.0 \times 10^{12} \text{ cm}^{-2}$ .

In the presence of the interface traps, the device performance degradation will occur caused by mobility degradation and surface potential degradation. An empirical model of inversion layer mobility has been developed as:

$$\mu = \frac{\mu_{eff}}{1 + KQ_{it}}, \quad (4)$$

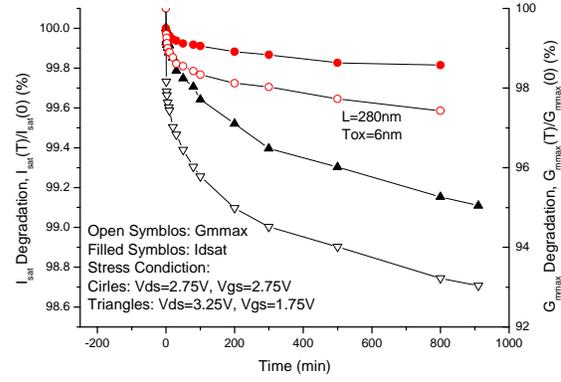


Figure 4:  $I_{sat}$  and  $G_{mmax}$  degradation versus stress time with different stress conditions.

where  $\mu_{eff}$  is the inversion layer mobility without interface trap ( $N_{it}=0$ ).  $K$  is a function of effective channel electric field,  $E_{eff}$ , which is empirically determined as [10]:

$$K = \frac{3.2 \times 10^{-12} \text{ cm}^2}{1 + (2.66 \cdot E_{eff})^{K1}}. \quad (5)$$

The degradation of drain current,  $\Delta I_d$ , in linear region has been developed as:

$$\frac{\Delta I_d}{I_d} = K \left( \frac{L_{it}}{L} \right) Q_{it}, \quad (6)$$

in which  $Q_{it}$  is assume to equal to  $N_{it}$ . Equation (6) has been extended to all regions. The degradation in drain current is proportional to  $KQ_{it}$ . Therefore, in subthreshold region, the drain current degradation will be less severe than that in strong inversion region due to  $Q_{it}$  being smaller in subthreshold region and saturated in deep strong inversion region.

### 3 RESULTS AND DISCUSSION

The  $I_{dsat}$  ( $I_{ds}$  at  $V_{ds}=V_{gs}=2.5\text{V}$ ) and  $G_{mmax}$  (maximum  $G_m$  at  $V_{ds}=0.1\text{V}$ ) degradation curve is shown in Fig. 4 with different stress conditions, filled symbols:  $V_{ds}=V_{gs}=2.75\text{V}$  and open symbols:  $V_{ds}=3.25\text{V}$ ,  $V_{gs}=1.75\text{V}$ . The  $I_{dsat}$  and  $G_{mmax}$  degraded more rapidly with the later stress condition due to the larger  $I_{sub}$ . A model predicting hot carrier induced linear current degradation due to interface trap generation is developed by James and Hu [10] and it is extended to saturation region in [11], in which the  $N_{it}$  reduction in saturation region is considered. However, in their model the lowering of the quasi-Fermi level, which decreases the total number of charge states caused by gate voltage, is overlooked. In this work, the relationship between total interface trap charge and gate voltage is studied. Figure 5 shows the percentage change in the drain current ( $\Delta I_{ds}/I_{ds}$ ) and change in drain current ( $\Delta I_{ds}$ ) versus gate voltage with different drain bias after 2000 minutes hot carrier stress. The  $\Delta I_{ds}$  increases with increasing gate voltage. However, the  $\Delta I_{ds}/I_{ds}$  behavior is different from

that of  $\Delta I_{ds}$ . It will increase in the low gate voltage region due to the  $Q_{it}$  being proportional to gate voltage in subthreshold region, and then reach the maximum around threshold voltage, after that it is reduced at increasing gate voltage since  $Q_{it}$  saturates to some value and  $K$  keeps decreasing as the electric field increases.

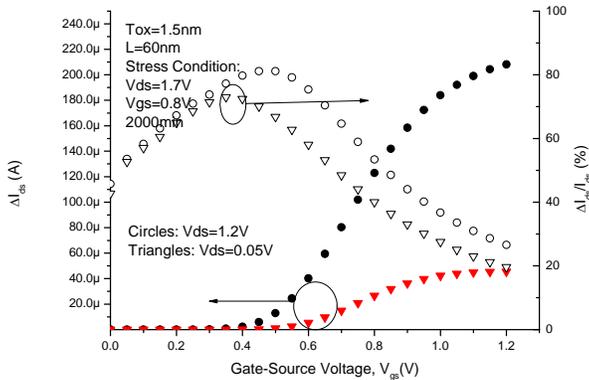


Figure 5: Drain current absolute and relative change versus gate voltage with different  $V_{ds}$ .

## 4 CONCLUSION

In this paper, we study the drain current degradation and transconductance degradation induced by hot-carrier stress. Interface traps are generated with hot-carrier stress and it can be monitored by measuring the substrate current. At a given interface trap density, the charge formulae of interface traps vary with different gate voltage. Therefore, the drain current degradation shows gate voltage dependence. In strong inversion region, the drain current degradation is more severe than in weak inversion region.

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