

Novel Low Temperature Fabrication Method for Label-Free Electronic Sensing of Biomolecules in Nanofluidic Channels with Integrated Electrodes

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ABSTRACT

We present a low temperature surface-micromachined fabrication process for creating centimeter long nanochannels with integrated electrodes. The maximum temperature of the entire process is kept below 300°C to allow for the integration of addressable electrodes for a variety of bioanalytical applications. The diffusion limit on the release etch length is overcome by releasing the channel structure along its length, decreasing the etch length from O(cm) to O(μm). In this work, we detail the fabrication steps and processes as well as discuss initial characterization and results.

Keywords: nanofluidic, fabrication, integrated electrodes

1 INTRODUCTION

The unique coupled physics inherent in nanofluidic systems has inspired much research towards the applications of biomolecule separation [1-4], sieving [5-6], and pre-concentration [7]. Compared to more conventional nanoporous systems, such as electrophoresis gels, microfabricated nanochannels provide better dimensional precision and control, resulting in new functionality and enhanced device performance [1-11]. Micro-/Nano-ElectroMechanicalSystems (MEMS/NEMS) fabricated nanofluidic channels allow for the incorporation of electronics embedded on the channels, which can be used to impart a surface charge on the channel [12], change the polarity for concentration enhancement [13], carry radio-frequency signals for sensing applications [14], and allow for exquisite temporal and spatial selectivity for the manipulation of biomolecules. Additionally, such channels allow us to study fundamental and unique coupled physics at the surfaces of substrates by providing in-situ sensing and potential control [12, 14]. Despite these promises, a key limitation in nanochannel research lies in the fabrication process.

The fabrication methods for such channels can be classified into two main categories: one which involves wafer bonding and one that uses a sacrificial release etch, as shown in Fig. 1. The bonding method offers process simplicity and has no limit on channel length since the channel is etched into one wafer and bonded into the other. However, this approach is limited to a single level and the

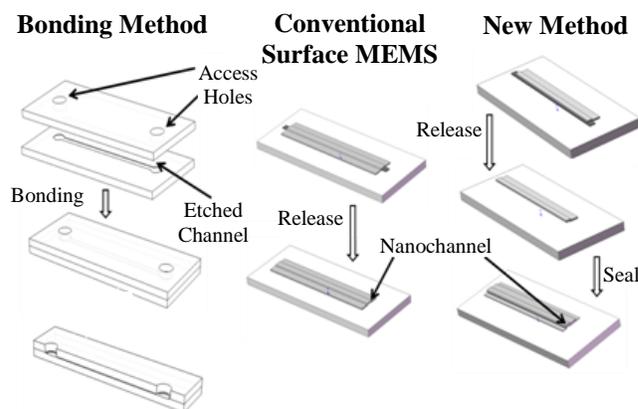


Figure 1. Comparison of different nanochannel fabrication methods. Left column shows the bonding method, in which channels are formed by trenches etched into a substrate and bonded to another substrate; Middle column illustrates the conventional surface MEMS approach: channels are created by release etch from channel ends; Right column highlights the newly proposed method: channels are released from the side and sealed by CVD.

process often demands either high temperatures (>1100°C for bonding for fused silica) [3-4] or the inclusion of adhesives as well as precise wafer alignment for bonding [15]. The sacrificial release method is based on surface MEMS techniques where the channels are formed by removing a thin sacrificial layer by wet chemicals, plasmas or chemical vapors. While wet chemical release provides good selectivity, the presence of liquids poses severe challenges on structural integrity and surface contamination [16]. Plasma release relieves the problem but is ineffective in removing materials without line of sight. Vapor release provides the advantages of both approaches. In particular, XeF₂ has been demonstrated to have superior selectivity between silicon and silicon dioxide [17]. However, removing sacrificial layers from long nanochannels remains a challenge due to the diffusion-limited long etching times described by the Deal-Grove model [17].

In this paper, we expand upon previously reported work [18] on a fabrication method for centimeter-long nanochannels by integrating metal electrodes into the process for on chip electronic detection. We demonstrate that this method can safely integrate metal layers, create centimeter-long nanochannels, and keep the temperatures

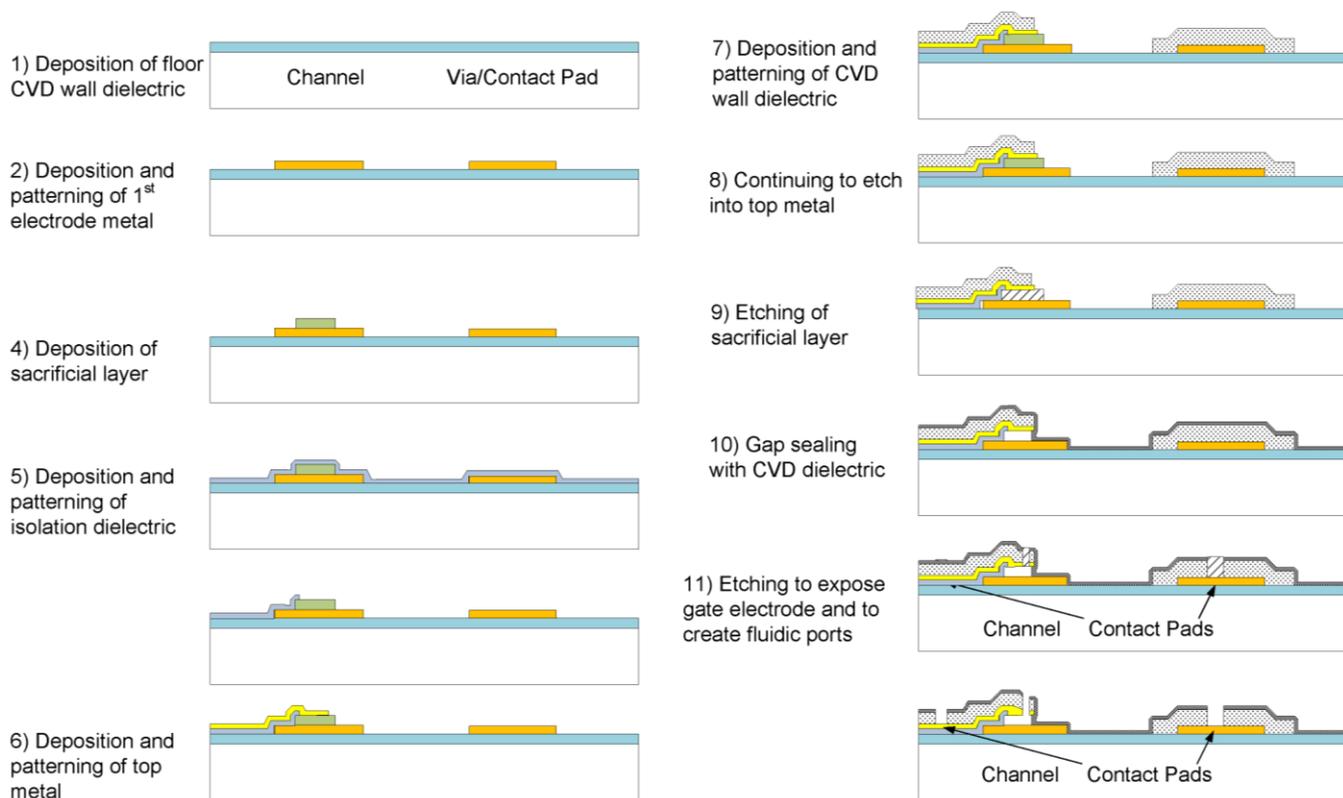


Figure 2. Process sequence for side-released nanochannels with integrated electrodes. Starting from a fused silica substrate, a layer of SiO₂ is deposited, followed by a layer of sputtered Cr-Au (patterned by liftoff); next an amorphous silicon layer is deposited and patterned. Next an insulating dielectric layer of SiO₂ is deposited and pattern, followed by a second Cr-Au-Cr deposition and patterning. Then another layer of SiO₂ is deposited and patterned. XeF₂ is then used to remove the amorphous silicon before sealing the channels with SiO₂. Finally, holes are etched at fluid ports to gain access to the channels.

Table 1. Typical deposition parameters for nanochannel process

Process name	Parameters
PECVD SiO ₂	SiH ₄ /O ₂ /Ar flow rates:7.5/15/20 sccm; Pressure: 5 mTorr; Power: Source=800W, Bias= 20W; Temperature: 100°C
PECVD SiN _x	SiH ₄ /N ₂ /Ar flow rates: 15.5/8.5/20 sccm; Pressure: 10 mTorr; Power: Source=800W, Bias=120W; Temperature: 100°C
PECVD a-Si	SiH ₄ / Ar flow rates: 15/20 sccm; Pressure: 1.5 mTorr; Power: Source=400W, Bias=35W; Temperature: 100°C
Post deposition annealing	250°C with 5°C/min ramping speed
Sputtered Cr	Ar flow 24 sccm, Pressure: 10 mT, Power 2 kW
Sputtered Au	Ar flow 24 sccm, Pressure: 10 mT, Power 2 kW

below 300°C at all steps. The resulting devices are compatible with CMOS processes and therefore a major step toward truly handheld devices.

2 FABRICATION

The key to this fabrication method is the formation of intermediate structures that are released on one side and the sealing step of the nanoscale gap with a CVD layer. The minimum lateral dimension of the resulting channels is determined by the lithographic step defining the lateral

edges of the channels and the amount of sacrificial material deposition in the thin channel gap.

The general fabrication process is illustrated in Fig. 2. The device substrate is a 525 μm thick, 100 mm diameter double side polished fused silica wafer (supplier: Hoya Corp.; model# 4W55-325-15C-STD), on which we deposit a 500 nm thick silicon nitride (SiN_x) layer with parameters shown in Table 1 by plasma-enhanced chemical vapor deposition (PECVD). After annealing the wafers at 300°C to stabilize the nitride film and reduce defects in subsequent depositions, a 50 nm thick layer of SiO₂ is deposited by PECVD which will act as the floor of the nanofluidic

channel. The metal electrodes are patterned using a 2-layer photoresist liftoff process with a sputtered Cr-Au-Cr stack. Next, 200 nm of sacrificial amorphous silicon (a-Si) and 20 nm of SiO₂ are deposited by PECVD. The thickness of the sacrificial layer determines the height of the nanochannel and the 20 nm SiO₂ layer forms the top wall of the nanochannel. Patterning of the sacrificial layer sandwich is done using CF₄/O₂ chemistries which etch SiO₂ anisotropically at ~150 nm min⁻¹ and a-Si at ~180 nm min⁻¹. A 50 nm thick layer of PECVD SiO₂ is deposited followed by a 1 μm thick PECVD SiN_x, both at 100°C. The SiO₂ and SiN_x layers form the channel wall materials and are subsequently patterned to expose the a-Si sacrificial layer by using a CHF₃-based etch. We then use pulsed XeF₂ vapor to release the channel through an isotropic etch. For XeF₂, the pulsing removes the gaseous waste of the etching reaction and a 60 s pumping time is implemented at the end of each etch cycle. The etch process has a > 1000:1 reported selectivity over SiO₂ [19-21] and is highly sensitive to moisture. For a 200 nm thick sacrificial layer and channel width of 5 μm, a single pulse of 90s each at 4 Torr was sufficient to complete the etching process. Next, we apply a high density oxygen plasma at 250°C to remove autofluorescence and change the surface of the channel from hydrophobic to hydrophilic for better compatibility with bioanalytical systems. These properties are a result surface fluorination caused by XeF₂.

At this point a gap is formed between the substrate and channel wall. The size of the gap is determined primarily by the thickness of the sacrificial layer and the stress gradient in the released films. A 500 nm thick PECVD SiO₂ layer (process parameters described in Table 1) is conformally deposited and seals this gap, thus completing the nanochannel. Finally, a CHF₃-based etch step is used to create access to the channel and the photoresist used to pattern the access holes is removed by O₂ plasma. Note that the channel is completely sealed during the last lithographic step, thus minimizing channel contamination.

3 RESULTS AND DISCUSSION

Previously we have completed and characterized, surface micromachined centimeter long nanofluidic channels without integrated metal electrodes [18]. In this work, we have completed fabrication of channels with electrodes, however, channels have not been completely released due to errors in the tolerances used to define the fluidic mask. Fig. 3 shows the introduction of a gate electrode into a nanofluidic channel, specifically an unsealed 7 μm wide nanogap with a 10 μm wide addressable gate electrode spanning the width of the channel. Errors in the tolerance of the features on the mask resulted in release lengths greater than 10 μm on the “cross geometry” features which resulted in nanochannels that were not complete, as shown in Fig. 4. Attempts at more cycles of XeF₂ failed due to the inefficiency of the diffusion limited process for long release lengths. Given the success

of our previous work [18], future work to complete these channels should be straightforward with better designed masks using the same conformal CVD sealing and CHF₃ fluidic access etch.

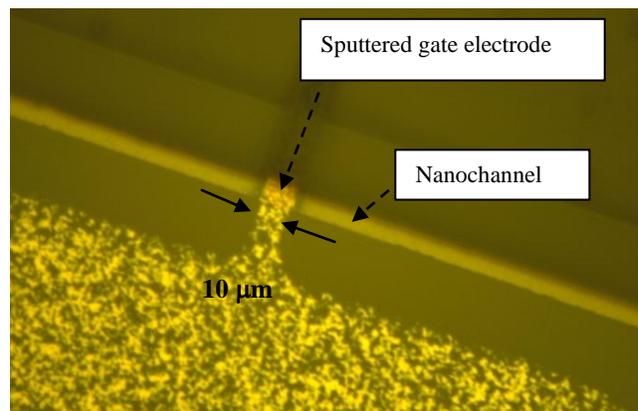


Figure 3: Nanochannel with integrated gate electrode. The introduction of gate electrodes do not interfere with the channel formation or lateral geometry

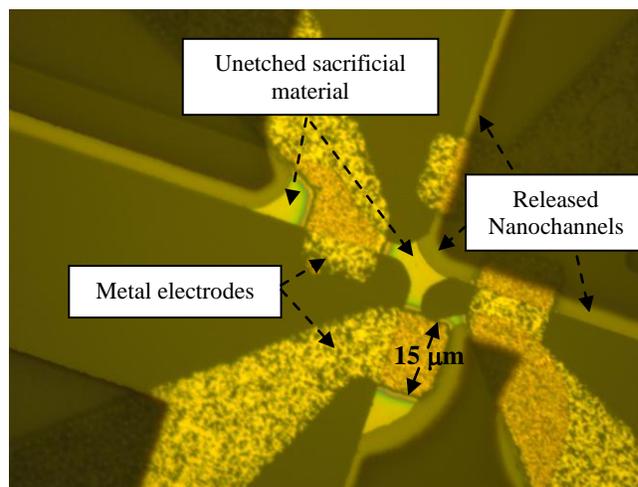


Figure 4: Cross channel geometry nanochannels not fully released due to tolerance errors in mask writing. This resulted in release lengths much greater than 7 μm. Arrows point to areas which are released as well as unetched sacrificial material and metal electrodes.

4 CONCLUSIONS

In this work, we have developed a low-temperature fabrication process for nanofluidic channels with integrated addressable electrodes. Compared to conventional methods, our process eliminates the maximum length limitation imposed by the Deal-Grove diffusion model. We explain our side release and CVD seal approach and discuss results to date. The low temperature process and dry release method have enabled integration of metals which can be used in a variety of bioanalytical applications.

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