Carbon Nanotube Field Effect Transistor (CNT-FET) 2-D Channel Electrostatic Potential Model for TCAD Application

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ABSTRACT

A 2-D channel electrostatic potential model of the CNT-FET that is shown in Figure 1 is presented. The model is developed by directly solving *Laplace's* equation in cylindrical coordinates with appropriate boundary conditions. Our mid-channel potential model is compared with the numerical results of [4] and it gives a good fit (see Figure 2). To the best of our knowledge, the Technology Computer Aided Design (TCAD) tool vendors have not provided models for CNT devices yet for the purpose of 2-D and 3-D device simulations. We believe the model presented in this paper may be useful for TCAD application.

Keywords: CNTFET, device modeling, device simulation, TCAD

1 INTRODUCTION

Aggressive scaling of the current CMOS devices technology significantly increases the device leakage power and short channel effects with each technology generation. The dimensional scaling of CMOS devices will eventually come to an end, currently predicted to be 2019 (see [1]). At the end of this roadmap, one of the alternatives to the current CMOS devices proposed by the International Technology Roadmap for Semiconductors (ITRS) is the Carbon Nanotube Field Effect Transistor (CNT-FET). It has been recently reported that a CMOS-analogous wafer-scale processing of integrated aligned nanotube circuits, wafer-scale synthesis and transfer of aligned nanotubes, metallic nanotube removal and chemical doping, and defect-tolerant integrated nanotube circuits has been successfully completed, [5].

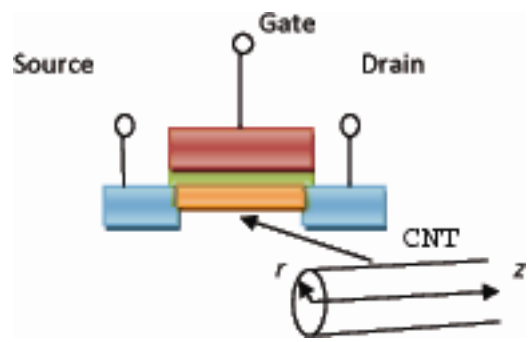

Fig. 1: Single-walled CNT field effect transistor.

In this paper we present TCAD compatible two-dimensional (2-D) channel electrostatic potential and surface charge density modeling results for a single-walled CNT-FET device. The models are developed by directly solving *Laplace's* equation in cylindrical coordinates with appropriate boundary conditions, as shown in Section 2. The device model simulation results and comparisons are presented in Section 3 (see Figures 2-8).

2 ELECTROSTATIC POTENTIAL MODEL

Assuming that a Schottky-barrier CNT-FET device is formed with an intrinsic nanotube in the channel, a piecewise electrostatic surface potential on $r=R_t$ from source (z=0) to drain (z=L) can be written as a function of z, [6, 7]:

$$V_S(z) = \begin{cases} \psi_{S1} = \psi_s - \dfrac{\psi_s}{(e^{\beta}-1)}[e^{\frac{-\beta}{a}(z-a)} - 1] & \text{for } 0 \le z \le a \\ \psi_S & \text{for } a \le z \le (L-a) \\ \psi_{S2} - \dfrac{\psi_s - V_{ds}}{(e^{\beta}-1)}[e^{\frac{-\beta}{a}(L-a-z)} - 1] & \text{for } (L-a) \le z \le L \end{cases} \quad (1)$$

where the Schottky-Barrier base width at the source and drain ends $a = 2(R_t + t_{ins})$, the barrier "concavity" measure $\beta = 3.6$, device channel length L, and R_t denotes CNT radius, t_{ins} dielectric thickness, V_{ds} source-drain voltage.

$$\psi_S(V_{gs}, V_{ds}) = V_{gs} - V_{fb} - \frac{k_b T}{q} W'\left(\frac{q^2 n_i}{2 k_b T C_{ins}} (1 + \alpha e^{\frac{-qV_{ds}}{K_b T}}) e^{\frac{q(V_{gs} - V_{fb})}{k_b T}} \right) \quad (2)$$

where V_{gs} denotes the gate voltage, V_{fb} the flat band voltage, n_i the intrinsic carrier density, k_b the Boltzmann constant, T temperature,

$$C_{ins} = \frac{2\pi\varepsilon_{ins}}{\ln(\frac{t_{ins}}{R_t} + 1)}$$ dielectric capacitance, t_{ins} dielectric thickness, ε_{ins} dielectric permittivity. *W'(x)* is the *Lambert* function which is a solution of $x = W' e^{W'}$ (see [9]). The parameter $\alpha = -13.8\bar{d}_t + 23.8$ is used as a fitting parameter and $\bar{d}_t$ is diameter of the nanotube per *nm* length.

A detailed derivation of the mid-channel surface potential (2) together with the channel charge density Q_{cnt} is given in [8, 3].

Solutions valid in the three separate domains of (1) can be joined or blended smoothly using a hyperbolic function (see [2])

$$V_S = \frac{(1 - \tanh(\gamma(z - L + a)))}{2} \left[\begin{array}{l} \frac{\psi_{S1}}{2}(1 - \tanh(\gamma(z - a))) + \\ \frac{\psi_S}{2}(1 + \tanh(\gamma(z - a))) \end{array} \right] \quad (3)$$

$$+ \frac{\psi_{S2}(1 + \tanh(\gamma(z - L + a)))}{2}$$

where the constant $\gamma = 10^{10}$ 1/*m*.

The electrostatic potential inside the nanotube is determined by solving *Laplace's* equation in 2-D cylindrical coordinates

$$\frac{\partial^2 V_0(z,r)}{\partial r^2} + \frac{1}{r}\frac{\partial V_0(z,r)}{\partial r} + \frac{\partial^2 V_0(z,r)}{\partial z^2} = 0 \quad (4)$$

with boundary conditions

$V_0(0,r) = \frac{-\phi_s}{q}, V_0(L,r) = V_{ds} - \frac{\phi_d}{q}$ and

$V_0(z, R_t) = V_S$, where q denotes electrical charge, ϕ_s source work function, ϕ_d drain work function and in this work $\phi_s = \phi_d = 0$ is used.

Exact solution of (4) with the above boundary conditions is

$$V_0 = \sum_{n=1}^{\infty} \left[\begin{array}{l} A_n I_0(\frac{n\pi r}{L}) \sin(\frac{n\pi z}{L}) + B_n J_0(\frac{x_{0n} r}{R_t}) \sinh(\frac{x_{0n} z}{R_t}) \\ + C_n J_0(\frac{x_{0n} r}{R_t}) \sinh(\frac{x_{0n}(L - z)}{R_t}) \end{array} \right] \quad (5)$$

where J_0 (x) and I_0 (x) denote the zero order *Bessel* and *Modified Bessel* functions respectively, the solution to J_0(x)=*0* is $x_{0n} \sim 3n\pi/4$, $A_n = \frac{2V_s(1-(-1)^n)}{n\pi I_0(\frac{n\pi R_t}{L})}$,

$B_n = \frac{2(V_{ds} - \phi_d/q)}{x_{0n}\sinh(\frac{x_{0n}L}{R_t}) J_1(x_{0n})}$, $C_n = \frac{-2\phi_s}{q x_{0n}\sinh(\frac{x_{0n}L}{R_t}) J_1(x_{0n})}$,

$\sum_{n=1}^{\infty} \frac{(1-(-1)^n)\sin(n\pi z/L)}{n\pi} = 1/2$ and $\sum_{n=1}^{\infty} \frac{J_0(x_{0n} r/R_t)}{x_{0n} J_1(x_{0n})} = 1/2$.

3 RESULTS AND DISCUSSION

Our modeling results are presented in this section. In Figure 2 the mid-channel potential model (2) is compared with the numerical results of [4] and it gives a good fit. Figures 3 and 4 show a good comparison for results of the piecewise potential, equations (1), with the blended form, equation (3). The 2-D simulation results of CNT-FET electrostatic potential (5) are given in Figures 5 and 6. The channel charge density profile with different source-drain voltages are shown in Figures 7 and 8.

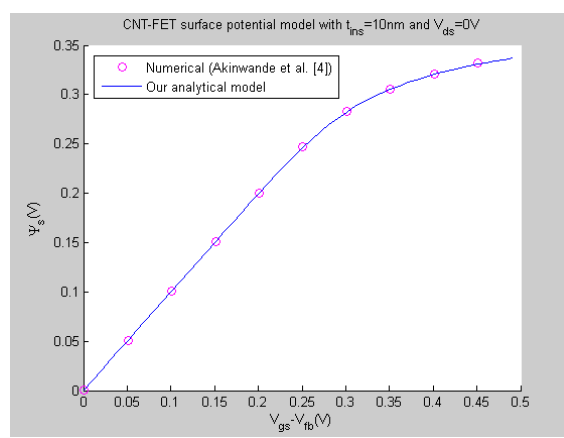

Fig. 2. CNT-FET mid-channel surface potential versus relative gate voltage V_{gs}-V_{fb} for nanotube diameter d_t=1nm, high-K dielectric thickness t_{ins}=10nm with K=15 is used.

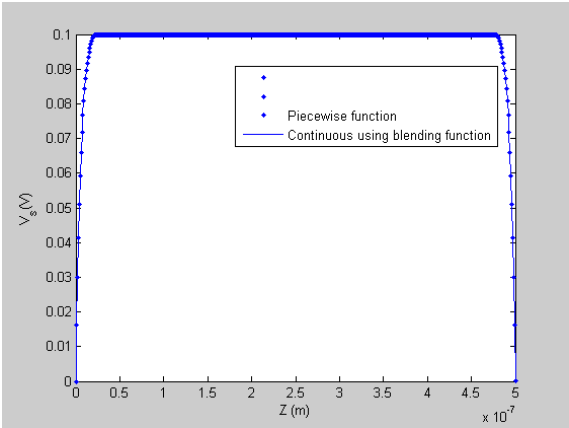

Fig. 3. CNT-FET source to drain channel surface potential profile with t_{ins}=10nm, d_t=1nm, L=0.5um, V_{gs}-V_{fb}=0.1V and V_{ds}=0V.

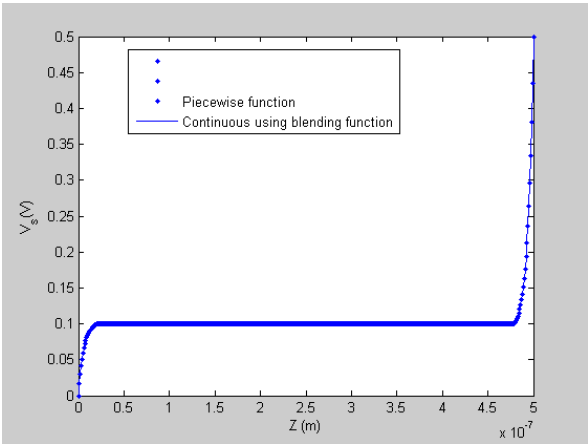

Fig. 4. CNT-FET source to drain channel surface potential profile with t_{ins}=10nm, d_t=1nm, L=0.5um, V_{gs}-V_{fb}=0.1V and V_{ds}=0.5V.

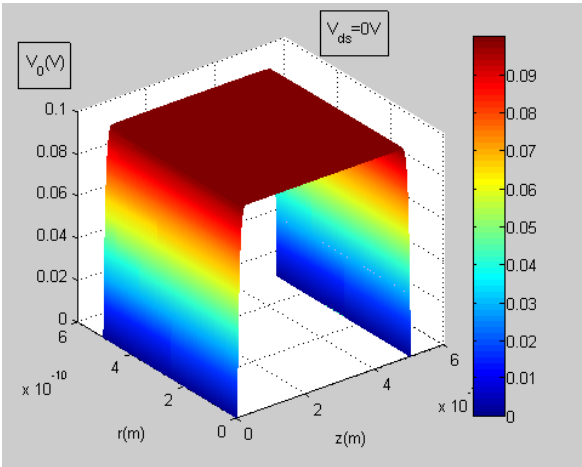

Fig. 5. CNT-FET channel electrostatic potential surface plot with t_{ins}=10nm, d_t=1nm, L=0.5um, V_{gs}-V_{fb}=0.1V and V_{ds}=0V.

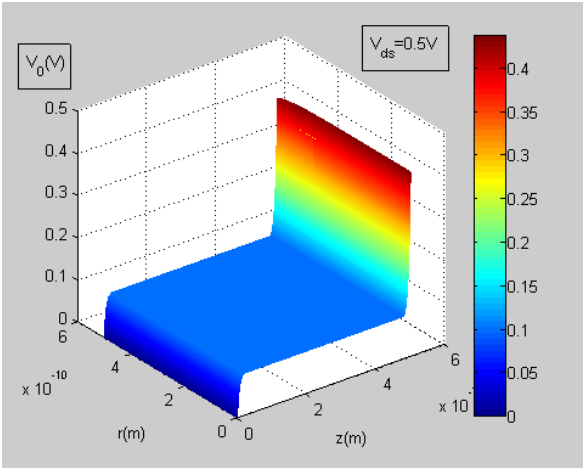

Fig. 6. CNT-FET channel electrostatic potential surface plot with t_{ins}=10nm, d_t=1nm, L=0.5um, V_{gs}-V_{fb}=0.1V and V_{ds}=0.5V.

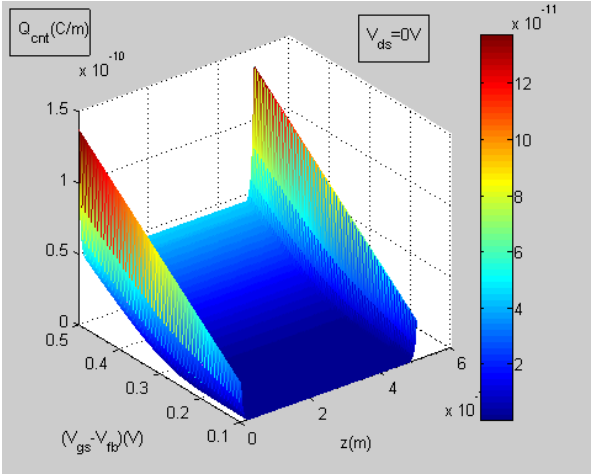

Fig. 7. CNT-FET channel charge density surface plot with t_{ins}=10nm, d_t=1nm, L=0.5um and V_{ds}=0V.

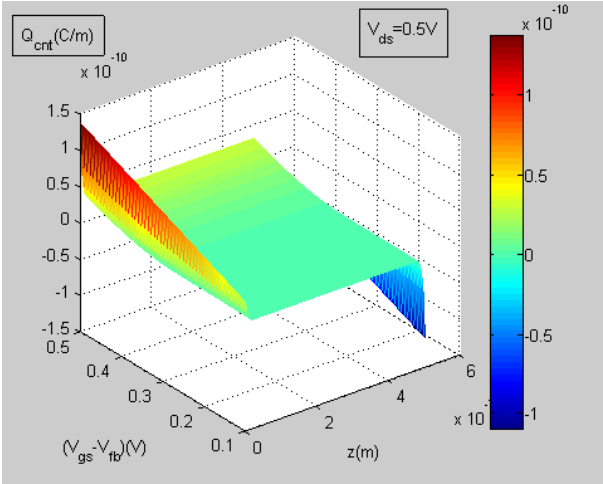

Fig. 8. CNT-FET channel charge density surface plot with t_{ox}=10nm, d_t=1nm, L=0.5um and V_{ds}=0.5V.

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REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS), Emerging Research Devices,(2005) http://www.itrs.net/Links/2005ITRS/ERD2005.pdf

[2] E. Cumberbatch *et al*., "Current-voltage characteristics from an asymptotic analysis of the MOSFET equations," *J. of Engineering Mathematics*, vol. 39, pp. 25-46, (2001).

[3] D. Akinwande *et al*., "An analytical derivation of density of states effective mass, and carrier density for achiral carbon nanotubes." *IEEE Tran. Electron Devices*, 55(1), (2008).

[4] D. Akinwande *et al*., "Analytical ballistic theory of carbon nanotube transistors: Experimental validation, device physics, parameter extraction, and performance projection." *J. Applied Physics*, 104(12), 124514, (2008).

[5] Koungmin Ryu *et al*., "CMOS-analogous wafer-scale nanotube-on-insulator approach for submicrometer device and integrated circuits using aligned nanotubes" *Nanoletters*, *ACS publications*, 9(1), 189-197, (2009).

[6] L. Castro *et al*., "Towards a compact model for Scottky-Barrier nanotube FETs." *Conference on Optoelectronics and Microelectronic materials & devices*, *COMMAD* 2002, pp. 303-306, Sydeney, Australia (2002).

[7] D. John *et al*., "Electrostatics of coaxial Schottky-Barrier nanotube field effect transistors." *IEEE Tran. Nanotechnology*, 2(3), (2003).

[8] H. Abebe *et al*., "Single-walled carbon nanotube field effect transistor device modeling." *Proc of the 2011 Nanotechnology conference*, June 13-16, (2011), Boston, MA.

[9] R. Corless *et al*., "On the Lambert W function", *Advances in Computational Mathematics* 5(4): 329-359 (1996).