3-state Quantum Dot Gate FETs in Designing High Sampling Rate ADCs

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ABSTRACT

The presence of quantum dots in the gate region of a quantum dot gate FET (QDFET) produces an intermediate state between the normal two stable ON and OFF states [1]. In this work we present Cadence simulation of 3-bit Analog-to-Digital Converters (ADCs) based on compact 3-QDFET comparators, using 32nm design rules with BSIM 3.2.0 and BSIM 3.2.4 models [3]. In addition, we present the precise control of the threshold voltage of variable threshold voltage transistor which will remove R-2R ladder problem in conventional analog-to-digital converters (ADCs).

Keywords: quantum dot, analog-to-digital converter, 3-state quantum dot gate FET

1 INTRODUCTION

The presence of quantum dots in the gate region of a quantum dot gate FET (QDFET) produces an intermediate state between the normal two stable ON and OFF states [1]. This "i" state is attributed due to a charge transfer from channel to quantum dots which result in a change in the threshold voltage over the range of gate voltage [2]. The range ΔV_{th} over which intermediate state occurs can be adjusted by device parameters. Recently, we presented usage of a QD gate nonvolatile memory as a variable threshold voltage FET and used it in conjunction with 3-state FETs to realize a comparator [3, 4]. The combination of a variable threshold FET along with two 3-state FETs make it useful for designing comparator circuits having different reference voltages.

In this work we present Cadence simulation of 3-bit Analog-to-Digital Converters (ADCs) based on compact 3-QDFET comparators, using 32nm design rules with BSIM 3.2.0 and BSIM 3.2.4 models [3].

2 DEVICE STRUCTURE

Figure 1(a) shows the cross-sectional schematic of a QD gate 3-state FET. Two layers of quantum dots are self assembled on the top of thin gate insulator between source and drain region. The difference of this structure with QD gate nonvolatile memory shown in Figure 2 is the absence of any control gate insulator on top of the quantum dots in the gate region. The transfer characteristics (Id-Vg) of a quantum dot gate FET is shown in Figure 1(b). Figure 1(b) shows that the drain current is independent of the gate voltage between 1.3V to 2.4 V of gate-to-source voltage. The transfer characteristic shows three distinct region of operation of QDFET.

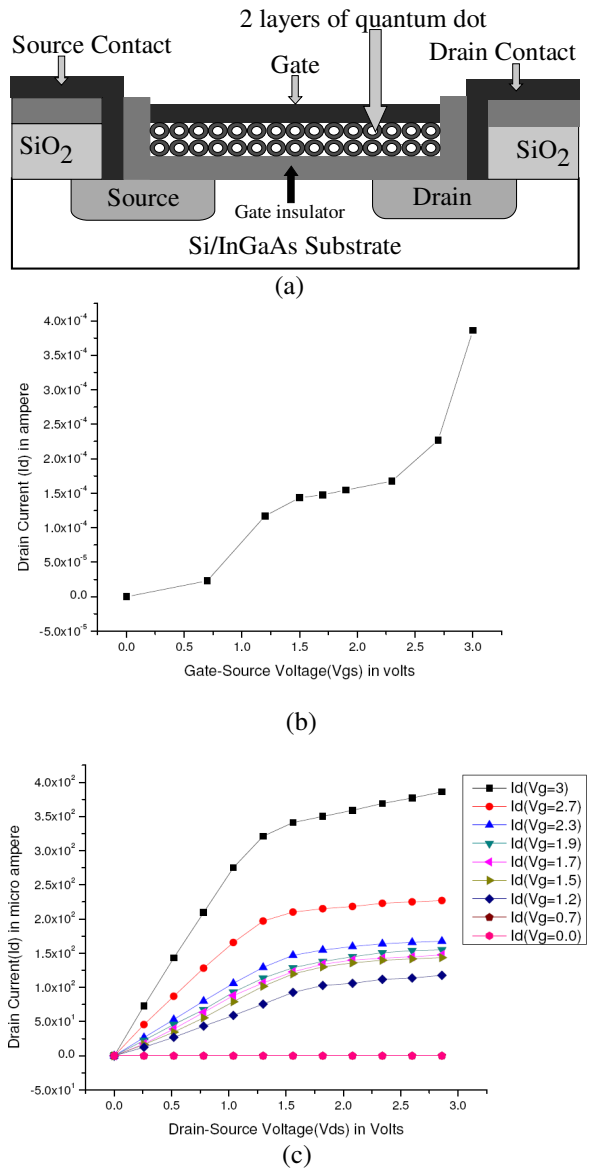


Figure 1: (a) Cross sectional structure of a quantum dot gate FET, (b) Transfer characteristics ($I_d - V_g$) of a fabricated

quantum dot gate FET, (c) Output characteristics ($I_d - V_d$) of a fabricated quantum dot gate FET.

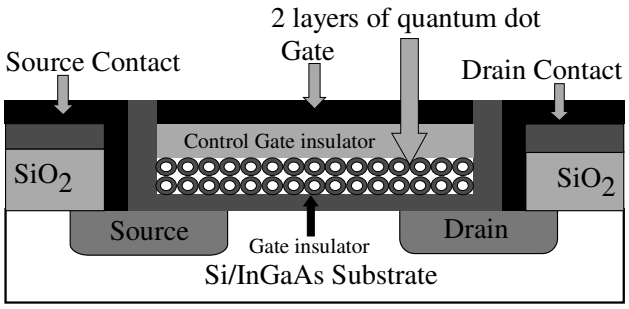


Figure 2: (a) Cross sectional structure of a quantum dot gate non-volatile memory.

3 CIRCUIT MODEL

The transfer characteristic of QDFET shows that it has three states: OFF, Intermediate and ON. The difference between conventional FETs and QDFETs is the presence of the intermediate state in the later one. In the intermediate state the drain current of the QDFET is independent of the gate voltage for a range of gate voltages.

In circuit model, we include intermediate state in terms of the threshold voltage change represented in equation 1. When the gate-to-source voltage (V_{gs}) is in between the lower threshold voltage (V_{g1}) and upper threshold voltage (V_{g2}), the effective threshold voltage has a term ($V_{gs} - V_{g1}$) which make drain current independent of the gate voltage in that region. Here α is a curve fitting parameter which varies from 0 to 1. When α is 1, drain current is independent of the gate voltage.

$$V_{Teff} = \begin{cases} V_T & V_{GS} < V_{g1} \\ V_T + \alpha(V_{GS} - V_{g1}) & V_{g1} < V_{GS} < V_{g2} \\ V_T + \alpha(V_{g2} - V_{g1}) & V_{GS} > V_{g2} \end{cases} \quad (1)$$

Figure 3 shows the transfer characteristics of the QDFET circuit model based on BSIM 3.2.0 using PTM 32nm parameters. The transfer characteristic shows the existence of intermediate state in the 32 nm feature size.

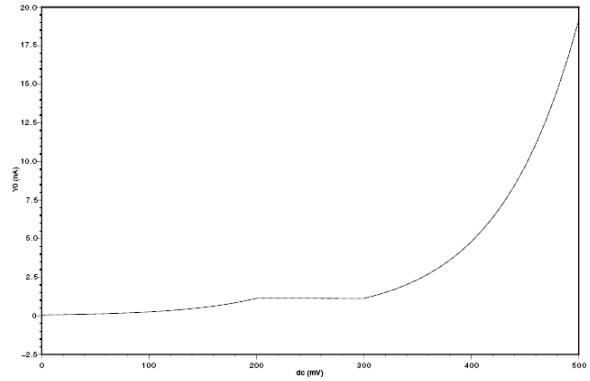


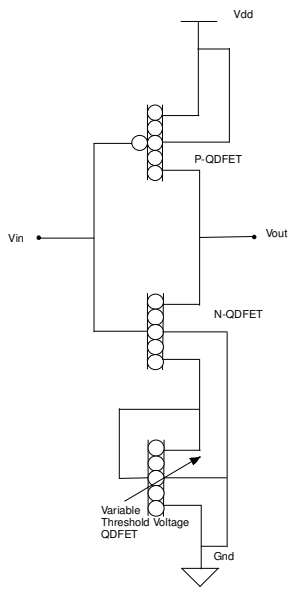
Figure 3: Transfer characteristics of the 32nm QDFET model.

	n-QDFET	p-QDFET
Mobility	0.03936 m^2/V-s	0.0035 m^2/V-s
Minimum L	32 nm	32 nm
Minimum W	32 nm	32 nm
$\mathbf{V_T}$	100 mV	100 mV
$\mathbf{V_{g1}}$	200 mV	200 mV
$\mathbf{V_{g2}}$	300 mV	300 mV
$\mathbf{V_{dd}}$	500 mV	500 mV
α	1.0	1.0

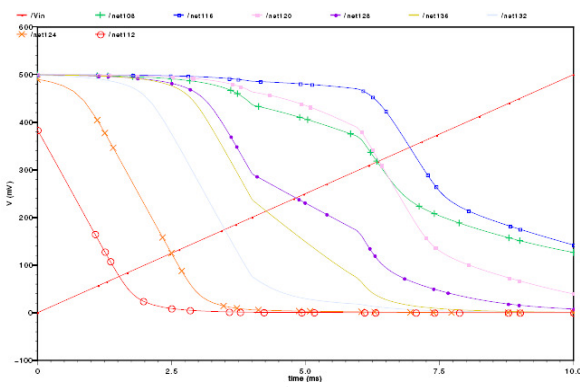
Table 1: Parameters for QDFET model

4 COMPACT COMPARATOR

Figure 4(a) shows the compact comparator circuit based on QDFET and quantum dot gate nonvolatile memory (QDNVM). This circuit is basically an inverter circuit having variable crossover point. The inverter circuit is designed based on the CMOS architecture where P-QDFET is used as a pull up transistor and N-QDFET is used as a pull down transistor. The variable crossover point is dependent on the variable threshold voltage transistor which is a QDNVM. The threshold voltage of QDNVM depends on the stored charge in the quantum dot layer in the gate region. In this circuit QDNVM act as a voltage dependent variable resistor. Threshold voltage variation of QDNVM changes the drain-to-source resistance of the device which changes the source voltage of the N-QDFET of the comparator circuit as well as the cross over point in the output. Figure 4(b) shows the variation of cross over point of the simulated comparator circuit.



(a)



(b)

Figure 4: (a) Comparator circuit diagram, (b) simulated output shows the variation of cross over point of the comparator

5 ANALOG-TO-DIGITAL CONVERTER

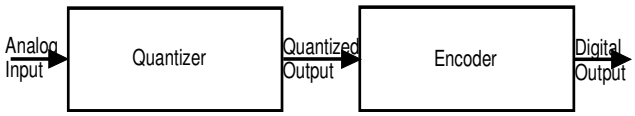
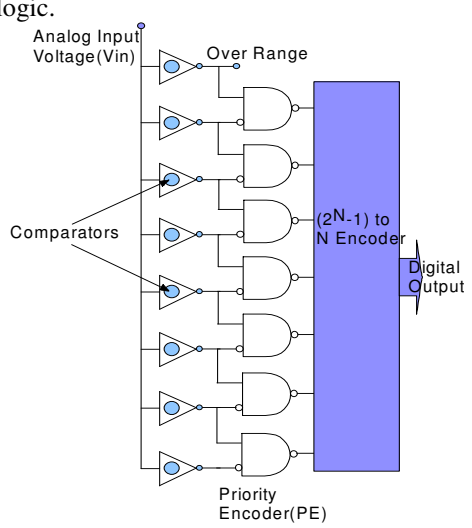
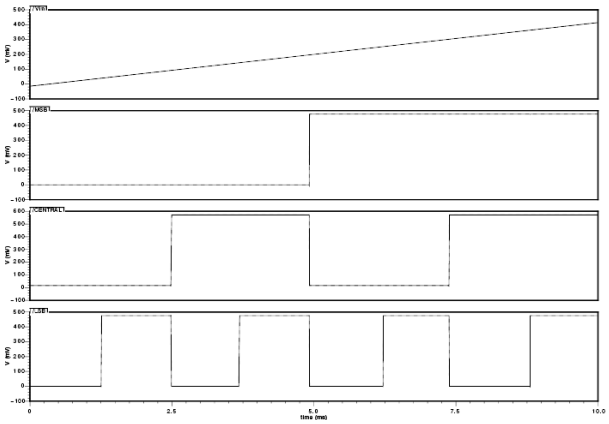


Figure 5: Block diagram of an analog-to-digital converter (ADC)

Figure 5 shows the block diagram of an analog-to-digital converter (ADC). The quantizer block, quantizes the analog input voltage in different quantized levels. The encoder converts the quantized voltages into different digital bit combinations. Figure 6 shows the flash architecture of the analog-to-digital converters (ADCs). We choose flash architecture because of relatively high speed of this architecture among all ADC architectures. In this architecture, the input analog signal is quantized into different quantized levels based on the different reference voltage of different comparators. In our QDFET based ADC circuit, we replace different comparators with compact comparator circuit based on QDFET and QDNVM discussed in section 4. Different reference voltages of different comparators are assigned by controlling the threshold voltage of the QDNVM of different comparator circuits. In the 32 nm architecture, we replace all long channel parameters by 32 nm parameters extracted from PTM model. We implement encoding in two stages. In the first stage, we extract the difference of consecutive comparator outputs. In the second stage we encode the consecutive comparator difference in different digital bit combination. In the encoder circuit we use BSIM v.3.2.0 model of MOSFET using 32nm PTM parameters. From the simulated characteristics in figure 6(b), it can be interpreted that because of nanometer range, the supply voltage decreases to 500 mV for 32 nm model. Similarly in the digital output, 500 mV is 1 and 0 mV as 0 according to positive logic.



(a)



(b)

Figure 6: (a) Flash architecture of 3-bit QDFET based Analog-to-Digital Converter (ADC) (b) Simulated output of a 3-bit Analog-to-Digital converter (ADC).

6 CONCLUSIONS

In this work we present Cadence simulation of 3-bit Analog-to-Digital Converters (ADCs) based on compact 3-QDFET comparators, using 32nm design rules with BSIM 3.2.0 and BSIM 3.2.4 models [3]. Existence of intermediate state in 32 nm design rule will make QDFET a promising circuit element in future. In addition, we present the precise control of the threshold voltage of variable threshold voltage transistor which will remove R-2R ladder problem in conventional analog-to-digital converters (ADCs).

ACKNOWLEDGEMENT

This work is supported by ONR Contracts N00014-02-1-0883 and N00014-06-1-0016, and NSF Grant ECS 0622068. Discussions with Dr. D. Purdy (ONR) and Dr. U. Varsheny (NSF) are gratefully acknowledged.

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