Carbon Nanotube Field Effect Transistors using Printed Semiconducting Tubes

N. Rouhi*, D. Jain*, K. Zand* and P. J. Burke*

*Department of Electrical Engineering & Computer Science, University of California-Irvine, California, USA, pburke@uci.edu

ABSTRACT

Purified, all-semiconducting nanotubes offer great promise for a variety of applications in RF and microwave electronics. It has been showed theoretically that carbon nanotube electronic devices have the potential of going into THz regime since 2004 [1]. In this work, we present device performance of thin-film transistors fabricated using a carbon nanotube spin-coating method that is economical and lends itself to mass manufacturing of nanotube electronics.

Keywords: carbon nanotube, high mobility, printed electronics

1 INTRODUCTION

Carbon nanotube devices have been speculated as having potentially THz cutoff frequencies since 2004 [1]. Since then, there have been many efforts to make this dream come true. However, only recently have the device cutoff frequencies crossed into the GHz range, as reviewed in [2]. To date, no RF devices with all-semiconducting nanotubes have been demonstrated. Both theoretical and experimental results show that having purified semiconducting tubes, as the channel of the transistor, will properly lead to desired Radio Frequency results. Study on different methods, such as dielectrophoresis, to deposit nanotubes, rather than in-place growth, have been a major focus of nanoelectronics recently [2]. Recent works also demonstrated a method of depositing self-sorted nanotube networks which can be used in fabrication of nanotube transistors [2].

In this work, we present progress towards RF devices using all semiconducting nanotubes as the starting material. A spin-on process, which is compatible with standard semiconductor processing, is presented.

The device performance is measured in an RF compatible electrode geometry. In addition, the DC measurements demonstrate high mobility (more than 30 cm^2/V-s) and good on/off ratio (in the range of more than 10^3 and 10^4 in some cases) achievements.

2 DEVICE FABRICATION

Devices reported here were fabricated using a solution enriched up to 90% in semiconducting single walled carbon nanotubes (Isonanotubes-S, semiconducting purity 90+, diameter range – 1.2-1.7 nm, length range 300 nm to 5 micron). These solutions were made using density gradient centrifugation process for the separation of nanotubes with different chiralities (n,m indexes) [3]. In the process, nanotubes were first dispersed in deionized water using ionic surfactants and then iodixanol, a non-ionic, water-soluble iodine derivative was added to the solution to be used as a density gradient medium prior to the separation based on centrifugation. For our experiments, we used nanotube's solutions as they were received without any further processing.

Prior to the deposition of nanotubes, Si/SiO2 wafers were first modified with APTES (Figure 1). An amine terminated self-assembled monolayer was formed after this modification to assist with the solution based deposition process. For this modification wafers with thin oxide layers were first treated with hot piranha solution for 1 hour and then washed thoroughly with DI water. Piranha treatment introduces –OH groups on the oxide surface. For forming a thin monolayer, piranha treated wafers were dipped into 1% APTES solution (v/v) in isopropanol. After an hour wafers were washed several times with isopropanol to remove excess APTES from the wafer surface and then they were dried by blowing air. Nanotube solution was then either spin-coated or a 20 μL nanotube solution was poured onto per sq cm of wafer. After letting it dry for an hour, wafers were washed with plenty of deionized water and then air dried prior to observing them on SEM (Figure 2).

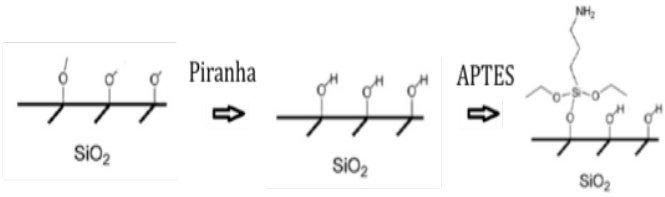

Figure 1: APTES treatment protocol.

Following the nanotube deposition, we patterned the wafer to deposit source and drain electrodes. The minimum

feature size on the mask is 5μm and the patterning process was done using the conventional photolithography by the means of MA-6 mask aligner.

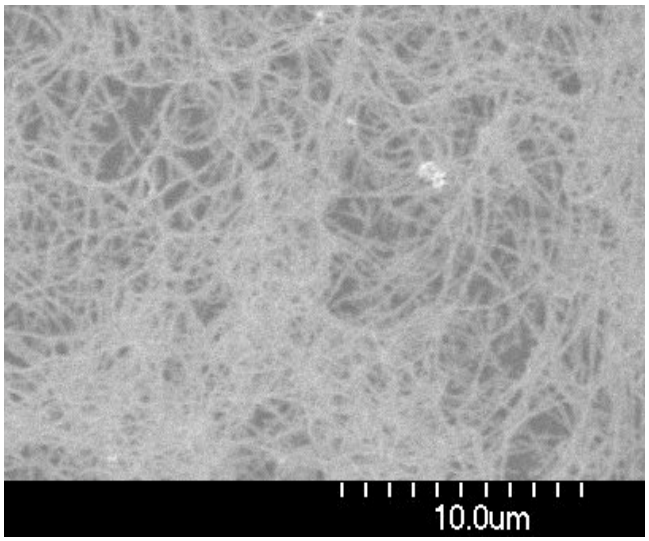

Figure 2: SEM image of nanotubes after deposition.

Gate lengths of 5~100μm (5μm and 10~100μm with 10μm increments) was designed to study the effect of gate length on the device characteristics. In all the devices, gate width is fixed and 200μm. After the patterning step, source and drain electrodes (30 nm Pd/ 100 nm Au) were deposited using e-beam evaporation followed by lift-off process. Palladium is used as the contact metal to nanotubes to make sure that the nanotube-metal contact is a resistive contact rather than Schottky. Devices were fabricated on Si substrate with 300nm high quality Silicon-dioxide cap and the Si wafer was used as the back gate. Figure 3 shows an SEM image of a fabricated device.

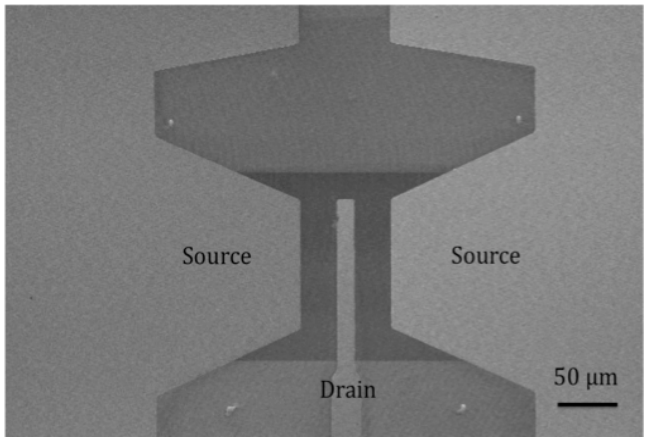

Figure 3: SEM image of fabricated device.

This design will allow for top-gate, three-terminal RF probing in the next generation of devices.

3 ELECTRICAL CHARACTERIZATION

The dc measurement data were extracted from devices with gate lengths of 5~100 μm and gate width of 200 μm. Figure 4 and 5 depict the current-voltage characteristic of one of the devices under DC bias.

The I_D-V_D curve is linear for V_D between 1 V and -1 V, indicating good ohmic contact between nanotube and electrodes as a result of depositing Palladium for the first layer on top of the nanotubes (Figure 4).

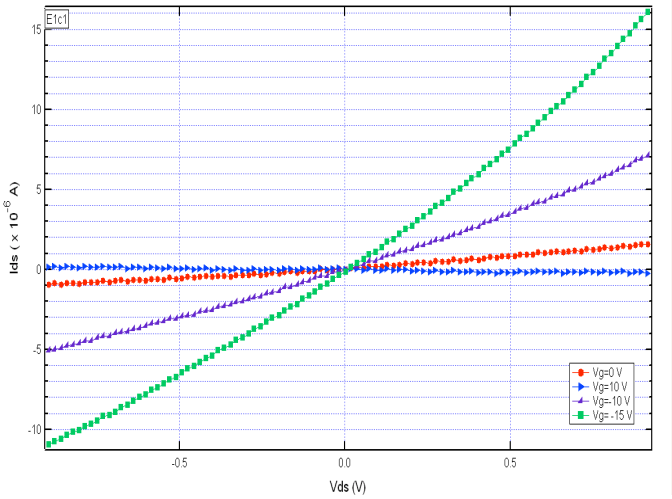

Figure 4: I-V characteristic (-1V < V_{DS}< 1V) showing the ohmic contact between electrodes and nanotube

By applying more negative V_D the devices clearly show saturation behavior (Figure 5).

The on/off ratio is more than 1000 in almost all devices. A reasonable assumption states that OFF current is roughly corresponding to the metallic nanotubes while both semiconducting and metallic tubes contribute in the ON current. Since we are using purified all-semiconducting (90% semiconducting) tubes in the channel, we are expecting high on/off ratio, which is true in our devices. In addition, the devices have a great p-type I-V curve response to the change in the back-gate voltage, which also is a result of forming the channel with semiconducting tubes. Gate voltage has been changed in the range of -10V to 10V with 2V increments.

Using the conventional I-V equations for MOS devices, we calculated the mobility by assuming the gate capacitance to be only the oxide capacitance.

$$\mu = \frac{L}{WCV_{ds}} . \frac{dI_d}{dV_g}$$

L is the length of the gate and W is the width that is fixed (200nm).

Mobilities more than 30 $cm^2/V\text{-}s$ was calculated using the above method and curve fitting the I_D-V_D characteristic while, taking the nanotube-substrate capacitance into account will make the total capacitance be less than the oxide capacitance therefore, resulting in higher mobility. These devices clearly show potential for RF performance when suitably optimized.

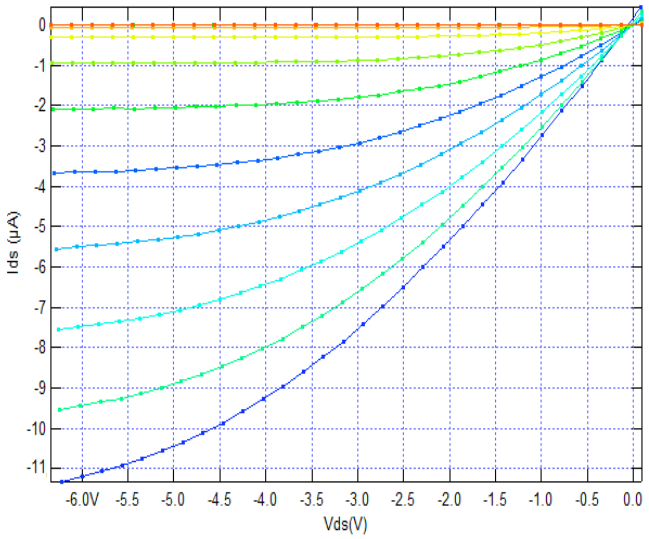

Figure 5: DC characterization showing the saturation behavior. (Vg varies from -10V to 10V with 2volts increment)

4 RESULTS AND CONCLUSION

In summary we reported thin film transistors fabricate using semiconductor-enriched carbon nanotubes. The APTES chemical treatment of the surface also allowed selective deposition of semiconducting nanotubes on the surface.

The dc electrical measurements show a great improvement in terms of mobility, current density and on/off ratio compared to previous works. Mobility of more than 30 $cm^2/V\text{-}s$ was obtained. Besides, on/off ratio of more than 1000 and perfect response to gate voltage (p-type I-V curve) will bring us to the conclusion that all-semiconducting nanotubes were deposited between the source and drain electrodes.

Pushing this technology into the microwave (GHz) range will require shorter gate lengths and higher mobilities. Since these are some of the first spin-on, all semiconducting nanotube devices ever made, these initial results are indeed quite promising for RF and microwave electronics.

ACKNOWLEDGMENT

This work was funded by the National Science Foundation, the Army Research Office, the Office of Naval Research, Northrop Grumman and the Korean National Science Foundation (KOSEF) World Class University (WCU) program.

REFERENCES

[1] P. J. Burke, "AC performance of nanoelectronics: towards a ballistic THz nanotube transistor" Solid State Electronics, vol. 48, pp. 1981-1986, 2004.

[2] C. Rutherglen, D. Jain, P. Burke, "Nanotube Electronics for RF Applications" Nature Nanotechnology, vol. 4, No. 11, 2009.

[3] M. Hersam, "Progress towards monodisperse single-walled carbon nanotubes", Nature Nanotechnology, vol. 3, no. 7, pp. 387-394,May2008.