Comprehensive Examination of Intrinsic-Parameter-Induced Characteristic Fluctuations in 16-nm-Gate CMOS Devices

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ABSTRACT

Intrinsic parameter fluctuations on device characteristic and yield are crucial in determining the operation of nanoscale semiconductor devices. In this paper, we examine the fluctuations of the threshold voltage (V_{th}), gate capacitance (C_g), and cutoff frequency (F_T) of emerging metal/high-κ gate planar complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs) variability including metal-gate-workfunction fluctuation (WKF), random-dopant fluctuation (RDF), and process-variation effect (PVE). An experimentally validated 3D "atomistic" simulation allows us to investigate the effect of aforementioned fluctuation sources on device DC/AC property. The preliminary results show that RDF and WKF dominate the device DC characteristics for n-type MOSFET (NMOS) and p-type MOSFET (PMOS), respectively. PVE affects CMOS device AC characteristics, especially at high gate bias.

Keywords: MOSFET, Characteristic fluctuation; Random-dopant fluctuation; Process-variation effect; Work-function fluctuation; Modeling and simulation

1 INTRODUCTION

The size of complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs) have been rapidly scaled down and the variability become a major challenge to device technologies. For state-of-art nanoscale CMOS circuits and systems, the intrinsic device parameter fluctuations that result from line-edge roughness, the granularity of the polysilicon gate, random discrete dopants [1-16], and other causes have substantially affected signal system timing [16] and high-frequency characteristics [15]. Yield analysis and power reduction, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and so forth, are known as indispensable components of circuit design. Diverse approaches have recently been presented to investigate and suppress the intrinsic-parameter fluctuations in semiconductor devices [4,5,14-16]. Among these approaches, the high-κ/metal-gate technology is the key to reduce the intrinsic-parameter fluctuations. However, the use of metal as a gate material introduces a new source of random variation due to the dependence of work function on the orientation of metal grains [17-20]. The change of CMOS device characteristics, caused by intrinsic device parameter variations, increased as the size is reduced; it may result in failure of integrated circuits with such small CMOS devices. Therefore, it is urgent to examine the intrinsic-parameter-induced CMOS device characteristic fluctuations.

In this work, organized as follow, we first propose the simulation methodology of intrinsic device parameter variability including the metal gate workfunction fluctuation (WKF), the process variation effect (PVE), and the random dopant fluctuation (RDF). Then we comprehensively investigate the intrinsic parameter variability induced threshold voltage (V_{th}), gate capacitance (C_g), and cutoff frequency (F_T) of fluctuations on 16-nm metal/high-κ gate n-type MOSFETs (NMOS) and p-type MOSFETs (PMOS). The results of this study show that RDF dominates the NMOS device characteristics, and WKF is major factor in PMOS. PVE affect the CMOS device AC characteristics, especially at high gate bias.

2 SIMULATION METHODOLOGY

The explored devices are the 16-nm-gate CMOS devices (width: 16 nm) with amorphous-based TiN / HfSiON gate stacks and an EOT of 1.2 nm. The nominal channel doping concentrations are 1.48×10^{18} cm^{-3} and the threshold voltage are 140 mV. To fairly compare the characteristic fluctuations and eliminate effects of the transistor size on the fluctuation, the same dimension, channel doping, and V_{th} are assumed for the 16-nm-gate NMOS and PMOS devices. Figures 1(a)-1(d) illustrate the RDF-induced fluctuation, the simulation mainly follows our recent work [9-17], in which 1310 dopants are randomly generated in a large cube of (96 nm)^3, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}. Then the large cube is partitioned into 216 sub-cubes of (16 nm)^3 and mapped into the device channel for the three dimensional (3D) device simulations with discrete dopants, as shown in Fig. 1(h). Notably, the maximum and minimum V_{th} are achieved for this specific set of 216 randomized channels would be different (larger range) if a larger number of samples were taken. Note that, comparing with a simulation of 1000 discrete dopant devices, the difference of the obtained
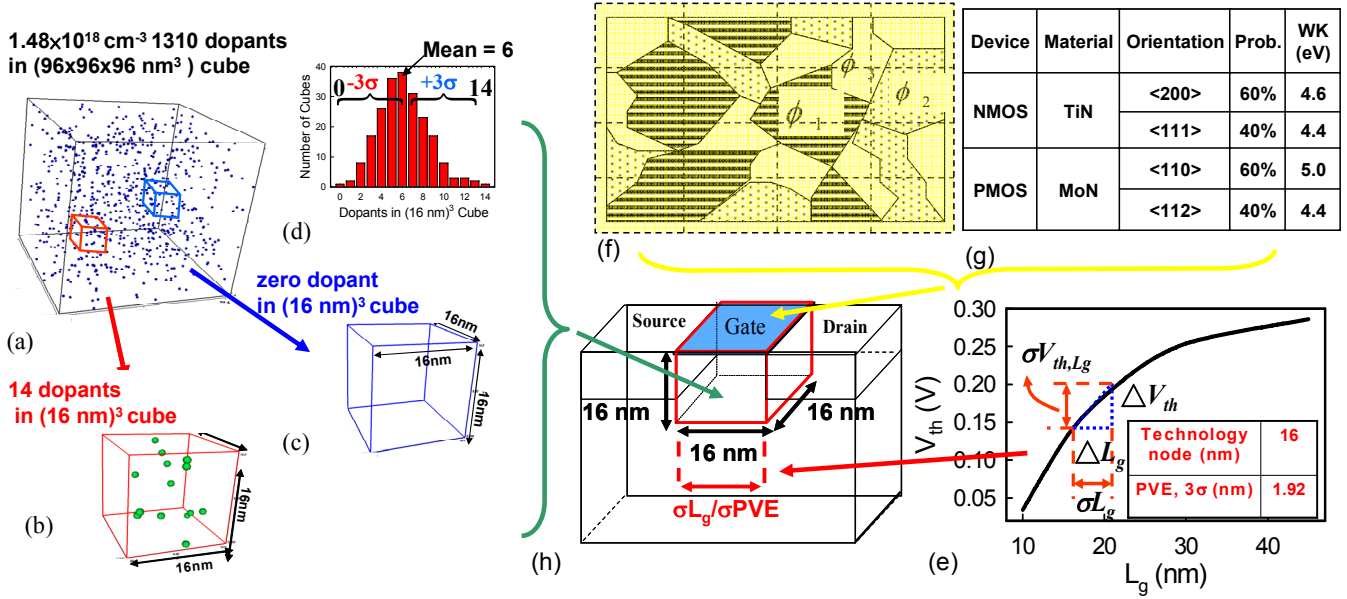
Figure 1: (a) 1310 dopants are randomly generated in a (96 nm)³ cube, in which the equivalent doping concentration is 1.48x10¹⁸ cm⁻³. The large cube is then partitioned into 216 (16nm)³ sub-cubes ((b)-(d)). (e) The magnitude of PVE follows the ITRS to estimate the PVE induced device fluctuations. (f) The gate area is composed of a small number of grains, and the estimation of WKF according to the metal properties in (g). (h) The explored 16 nm planar MOSFETs for 3D simulation.

threshold voltage fluctuation (σV_{th}) for the set of fluctuation sources of device characteristics variations are 216 randomized devices is only 1 mV. Therefore, the major fluctuation sources are the same. The PVE in this work include the gate length deviation and line edge roughness. We assume the magnitudes of PVE are Gaussian distribution and follow the projection of ITRS [22], as shown in Fig. 1(e). For WKF in Fig. 1(f), a Monte-Carlo approach is proposed for examining such effect, the gate area is first partitioned into several parts. Then, the workfunction of each partitioned area is randomized following the properties of metal in Fig. 1(g) [18, 19]. The effective workfunction of single device is the average of all partitions and uses for estimation of WKF-induced characteristics fluctuations. There are 200 devices generated for PVE and WKF, respectively. The physical model and accuracy of simulation approach have been quantitatively calibrated by experimentally measured results [10].

3   RESULTS AND DISCUSSION

Figures 2(a) and 2(b) show σV_{th} for NMOS and PMOS, respectively. The total V_{th} fluctuation, $\sigma V_{th,total}$, according to the independency of the fluctuation components, is given below,

$$\sigma_{V_{th,total}}^2 = \sigma_{V_{th,RDF}}^2 + \sigma_{V_{th,PVE}}^2 + \sigma_{V_{th,WKF}}^2 , \qquad (1)$$

where $\sigma V_{th,PVE}$, $\sigma V_{th,WKF}$, and $\sigma V_{th,RDF}$, are the RDF-, PVE-, and WKF-induced V_{th} fluctuations. From simulation results,
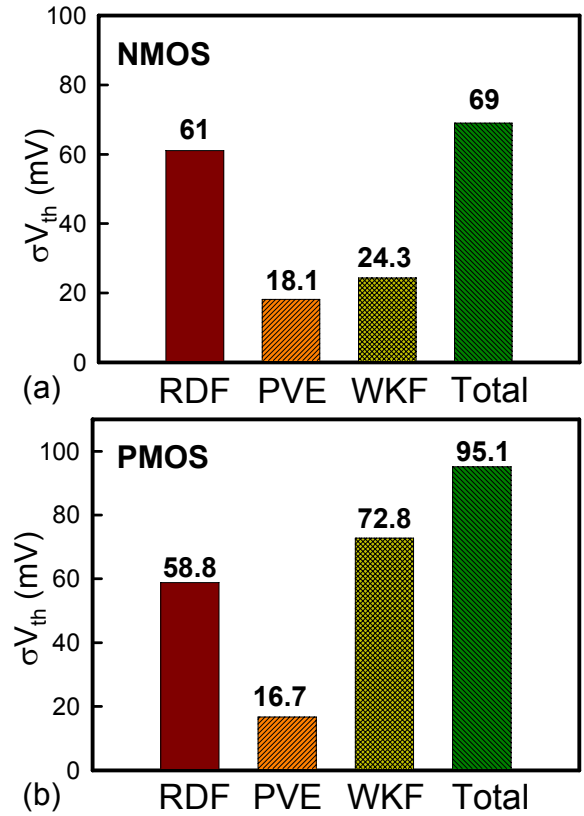
Figure 2: The threshold voltage fluctuations induced by intrinsic parameter variations for the 16 nm (a) n-type and (b) p-type planar MOSFETs.
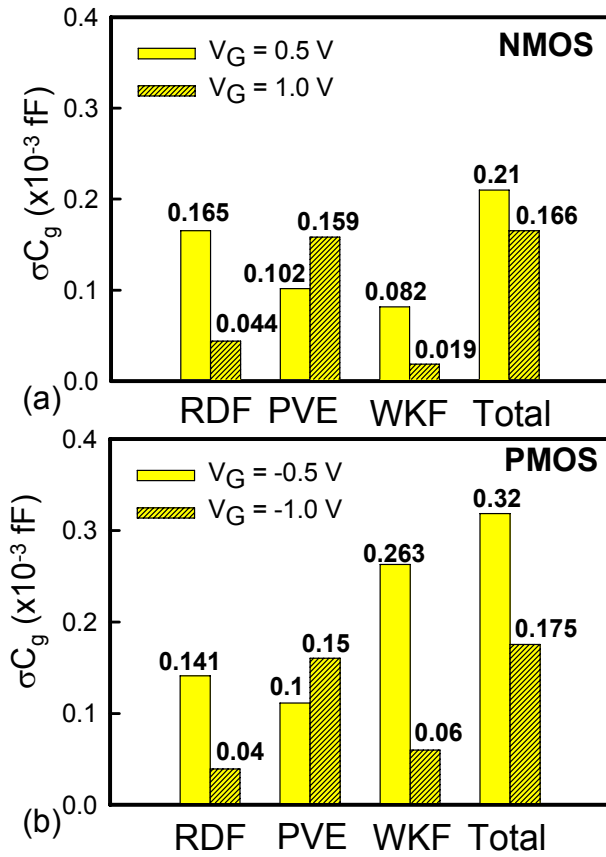
Figure 3: The gate capacitance fluctuations induced by intrinsic parameter variations for the 16 nm (a) n-type and (b) p-type planar MOSFETs.
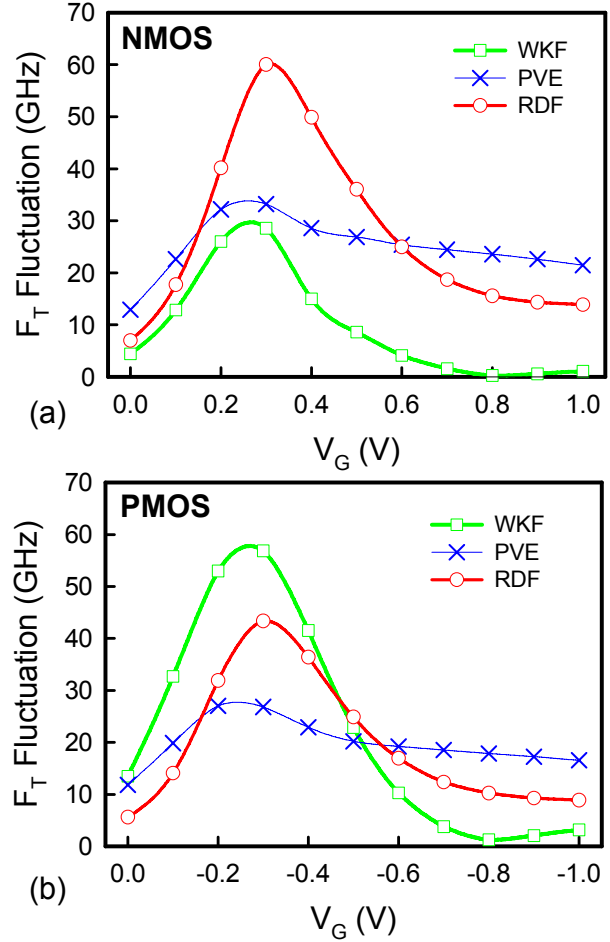

Figure 4: The cutoff frequency fluctuations induced by intrinsic parameter variations for the 16 nm (a) n-type and (b) p-type planar MOSFETs.

the random-dopant fluctuation dominates the fluctuation of V_{th} in NMOS. However, for the fluctuation of V_{th} in PMOS, the workfunction fluctuation becomes the dominating factor because of the large deviation of the workfunction for different orientation of metal grains. The total threshold voltage fluctuations for NMOS and PMOS are 69 mV and 95 mV, respectively.

Figure 3 shows the gate capacitance fluctuations (σC_g) for NMOS and PMOS at $V_G = 0.5$V and 1V. Similarly, the total gate capacitance (C_g) fluctuation, $\sigma C_{g,total}$ is given,

$$\sigma_{C_{g,total}}^2 = \sigma_{C_{g,RDF}}^2 + \sigma_{C_{g,PVE}}^2 + \sigma_{C_{g,WKF}}^2 \,, \qquad (2)$$

where $\sigma V_{Cg,PVE}$, $\sigma V_{Cg,WKF}$, and $\sigma V_{Cg,RDF}$, are the RDF-, PVE-, and WKF-induced C_g fluctuations. The results are similar to the results of σV_{th} at low gate bias ($V_G = 0.5$V), RDF and WKF are dominate variation sources. However, the RDF and WKF brought less impact on σC_g due to the screening effect of the inversion layer at high gate bias ($V_G = 1$V). The screening effect isolates the variation of surface electrostatic potential and decreases the σC_g. The PVE gives

sizeable impact on the gate length and is independent of the screening effect, which should be noticed when the transistor operated at high gate bias.

Figures 4(a) and 4(b) illustrate the intrinsic parameter fluctuation induced cutoff frequency fluctuations (σF_T) as a function of gate voltage for NMOS and PMOS, respectively. The cutoff frequency (F_T) is calculated as below:

$$F_T = v_{sat} / 2\pi L_g = g_m / 2\pi C_g \,. \qquad (3)$$

The simulation results show that RDF and PVE are important in NMOS at low and high gate bias, and the impact of WKF can be neglected. In PMOS at low gate bias, besides the WKF, RDF is still also a major variation source, and PVE is important at high gate bias, which similar to the results of σC_g. All the RDF, PVE, and WKF should be carefully considered in PMOS' AC characteristics.

4 CONCLUSIONS

In this paper, we have comprehensively explored the impact of intrinsic parameter fluctuations, WKF, PVE and RDF on DC and AC characteristics' fluctuation for 16-nm-gate planar CMOS devices. By experimentally validated three dimensional atomistic simulation, RDF and WKF dominate the device DC characteristics for NMOS and PMOS, respectively. For AC characteristics, the RDF and PVE are important in NMOS at low and high gate bias, and the impact of WKF can be neglected. In PMOS at low gate bias, besides the WKF, RDF is still also a major variation source, and PVE is important at high gate bias. All the RDF, PVE, and WKF should be carefully considered in AC characteristics of PMOS.

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