An SOA Aware MOSFET Model for Highly Integrated, Analog Mixed-Signal Design Environments

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ABSTRACT

Circuit simulations involving power devices often require additional checks comparing with generic low power applications. The burden lies with the individual designers to ensure that the power transistors are operating well within the Safe Operating Area (SOA) and EOS (electrical overstress) limits. However, it is not trivial to perform such checks due to the inherit limitations of industry standard MOS models: inadequate diode model for the junctions, non-existence of junction breakdowns, and alert when such breakdown voltages are reached. In this paper, we have created a BSIM3 subcircuit-based POWER MOSFET Model with a behavioral current source conforming to the SOA contour extracted from the pulse measurements. An additional warning system built-in to the Cadence *Spectre* Simulator, the designer will be able to catch both transient spikes and dynamic breakdowns (function of V_{gs} and V_{ds}) outside of the SOA of the Power MOSFET; both by an output logfile of circuit nodes and the associated time intervals where they are outside of the SOA region, and visually where the breakdown anomalies are observable due to the behavioral current source within the subcircuit model. This methodology can be easily generalized to other devices for the circuits of interest.

Keywords: power, analog, breakdown, safe operating area, electrical overstress

1 INTRODUCTION

Power and high-voltage MOSFET transistors and power circuits are becoming much more prevalent in integrated circuit design. Previously, these MOSFETs were strictly manufactured as discrete transistors and simulations were single device based and the devices were integrated at the printed-circuit board level. With the world advancement of semiconductor processing and the push for power electronics to be ever smaller, the implementation of monolithic circuits with power transistors and standard integrated circuit components has become a major growth area in analog electronics.

Traditional circuits such as logic, small-signal and most analog applications do not operate in regions where the limits of the process can be tested. However, power and high-voltage transistors often operate at the limits of the their technologies and therefore making sure the devices remain within the bounds of the process is critical in silicon design. Traditionally, it has been dependent upon the designer to check the critical pins for transient voltage violations. This process is very tedious and relies on the designer to know which nodes to check. Also, as the size and complexity of power integrated circuits increases, this checking becomes unbearable, so an automated method of checking is needed.

Current EDA tools have begun to recognize this need for device checking so they have implemented some basic aspects of this checking. Most of the development has been on "node" checking rather than individual device checking. Cadence has introduced a tool into the Cadence Analog Design Environment that allows for setting individual parameters at the device level and then produce a report at the end of the simulation of violations. This tool can only check individual voltages and currents. Power and high-voltage devices often do not have traditional "operating" boundaries. This limitation put some constraints on traditional SOA and EOS checking. We modify the device checking of the Cadence and include additional elements and equations to properly map the SOA of these devices.

2 SAFE-OPERATING AREA (SOA)

2.1 Voltage limits and the SOA contour

Traditionally, process development guidelines place hard limits (often very conservative) for SOA or EOS on MOSFET device operation. So, for a traditional 5-V CMOS process, the device engineer may place absolute limits of 5.5-6.5 volts for Vgs and Vds on standard CMOS transistors, and it is quite easy to see if one falls outside these guidelines. However, for power and high-voltage transistors, there are often transients that can result in the Vgs and Vds exceeding these boundaries. Also, depending upon device layout the bulk resistance can play a part in the absolute maximum voltage that a device can withstand. The voltage limits now for the Vds and Vgs are no longer "fixed" and are dependent upon many parameters such as device size, biasing, layout geometry, etc.

The standard device checking is insufficient for these complex voltage limits. The limits form what is called a Safe Operating Area contour.

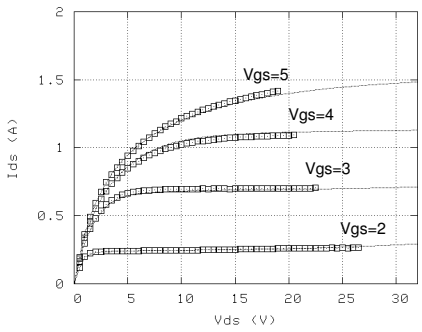

Figure 1: Id-Vd Family of Curves for High-voltage MOSFET. Symbols are measured data.

Looking at the traditional Id vs Vd family of curves above for a high-voltage NMOS device, one can see that the device fails at different Vds values depending on the Vgs value. As the Vgs increases, the Vds limit decreases.

2.2 Predicting SOA breakdown

Another issue with traditional MOSFET simulations is the limited ability to predict device breakdown. Standard diode models usually include some breakdown parameters as does some MOSFET devices, however, these are usually "hard" numbers. Looking at the SOA contour, one would like to create a model that creates a breakdown that is dependent upon the applied gate and drain voltages so that the device can accurately predict breakdown when the device violates its limits. This model should also be easily integrated as an extension to existing models so that it can be turned on and off to improve simulation time.

We developed a behavioral model subcircuit that can predict the breakdown depending upon the applied voltages, device size, temperature, etc.

3 SOA/EOS AWARE MOSFET MODEL

We developed our model from a manufactured integrated extended-drain MOSFET device. The device is a large MOSFET (W>1mm). We will use measured data from this device to compare with our predictive model. The values presented here are "normalized" for simplicity.

To develop our SOA aware model, we used our traditional approach to high-voltage MOS modeling using a standard BSIM model and extended drain resistor that is voltage dependent. We also include gate, source, and drain resistances and use a stand-alone drain-body diode for better parasitic modeling.

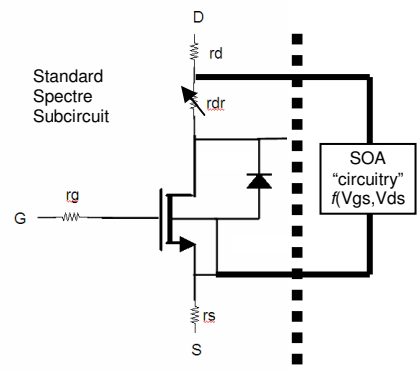

Figure 2: High-voltage MOSFET model with SOA "Aware" circuitry.

With the advent of complex behavioral modeling we are able to create an "SOA Aware" subcircuit that consists of behavioral elements which monitor the device operating parameters. This circuit will then map the contour of the device under test and properly report violations of the SOA for the device as well as predict "breakdown" at the correct Vds voltage depending on the Vgs voltage. Additionally, we did many "stress" tests on the model to ensure that there were no convergence issues.

4 MODEL TEST AND VALIDATION

4.1 DC testing

The testing of the DC included verifying the SOA model was functional, created the proper warning messages at the correct voltage values and properly simulated breakdown. We used a pulsed DC measurement system to capture the Ids-Vds family of curves for our DUT. (see Fig 1). Figure also shows the traditional DC simulation without the SOA contour such that the MOSFET current continues to simulate "normally" even though the device has reached its SOA limit. In Figure 2, we apply our SOA Aware model to the HVMOS macromodel. One can now see that at each respective Vgs voltage the device hits "breakdown" and there is a simulated breakdown in the model.

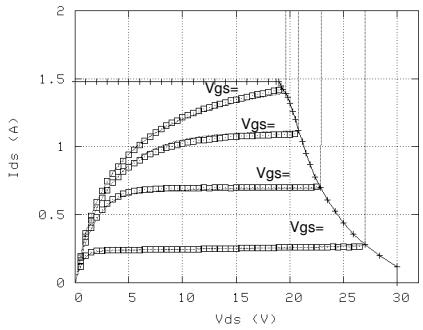

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Figure 3: Id-Vd Family of Curves for High-voltage MOSFET. Symbols are measured data.

Cadence also creates a report file showing the violation occurrences in the device. (See Figure 6 at the end of the paper.) The report correctly predicts the Vds SOA voltage point for each different Vgs.

4.2 Transient testing

The true value of the SOA Aware model is in the transient simulation. The transient simulation is where devices can see small (or large) spikes in short periods of time that are difficult to catch visually in device checking. Also, the transient is closest to the transistor operating in its "natural" state for applications. Many power circuits include inductive and capacitice elements that can create over and under voltage spikes, fast current increases, etc., any of which can create unexpected voltages on transistors.

To test our SOA aware model we used a sample power output circuit that includes L, R and C elements. We also used the device in such a way that we would get unusually voltages on the Vds to properly check the operation of the SOA subcircuit.

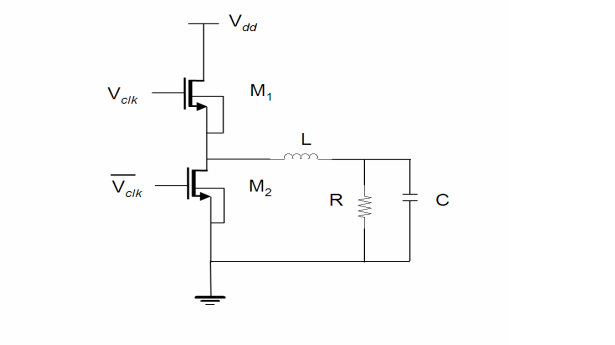

Figure 4: Sample transient test circuit for SOA model. The M1 transistor is the DUT.

For our simulation, we created a clock signal for the *Vclk* and *Vclk'* pins. We then created a slowly ramping Vds voltage. As predicted as the voltage Vds voltage ramped, when the device exceeded the recommended SOA voltage, a "breakdown" is clear in the simulated results. One can also see the traditional model simulation will not simulate the breakdown and create an output that looks to be typical and not problematic. Again, in this case, the Cadence system also created a violations output file (see Fig 7). The nice thing about the violation output file is that it shows exactly the time that the device exits the SOA and then re-enters. This information is useful is predicting how "bad" the circuit is violating the recommended limits as well as can give the designer clues to what particular circuit elements or signals are causing the violations.

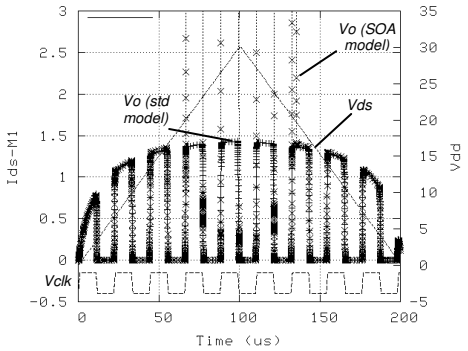

Figure 5: Transient output of power output stage using standard and SOA MOSFET models.

5 CONCLUSIONS

We developed an extension to traditional power and high-voltage models that can accurately predict that the device is operating within the recommended limits for the device. This additional element consists of behavioral model elements that are geometry and bias dependent. Due to its behavioral nature, it is easy to extend this model to include temperature, layout, and other parameters if they are necessary for predicting device SOA.

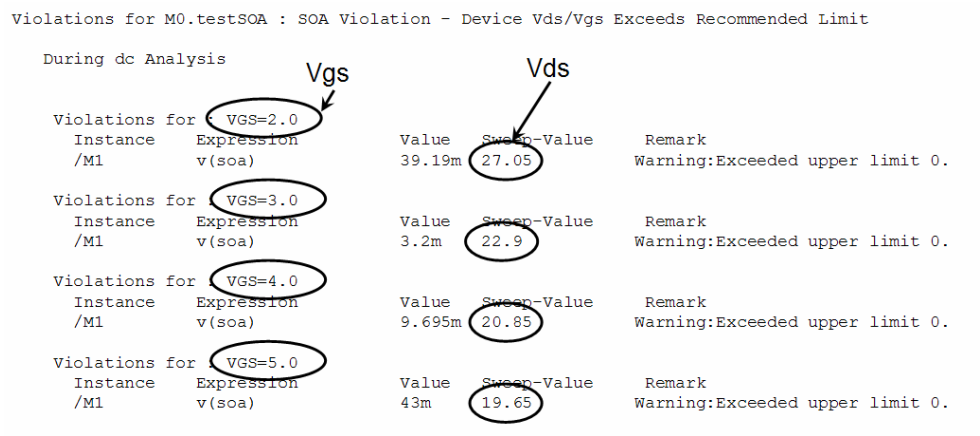

Figure 6: Violation output report for DC simulation.

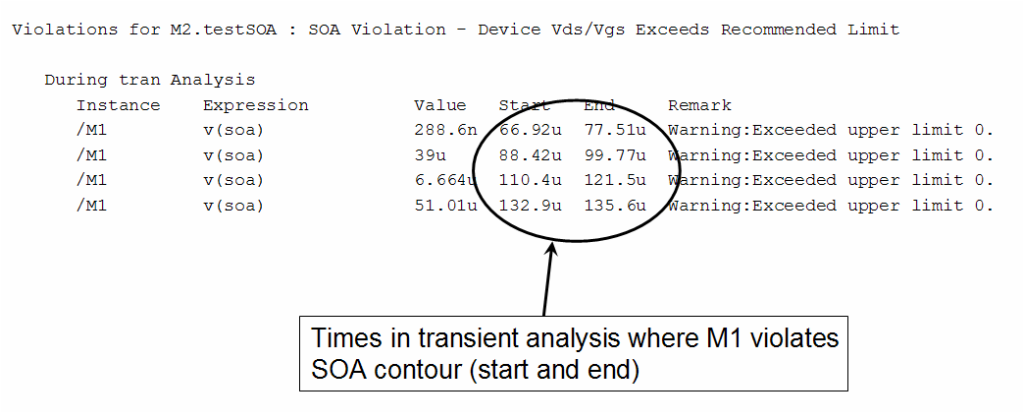

Figure 7: Violation output report for Transient simulation.