Source/Drain Junction Partition in MOS Snapback Modeling for ESD Simulation

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ABSTRACT

An enhancement to the modeling of the 'snapback' in MOS transistors for ESD simulation is presented. The new model uses industry standard models and includes all major physical effects characteristics of snapback. The MOS snapback model is enhanced by partitioning the Drain and Source junctions so that only a portion of them is included in the parasitic BJT. The comparison of simulation and measured data of a Grounded-Gate NMOS shows good agreement for both positive and negative drain voltage stresses. Simulation of the base current of the parasitic bipolar shows significant improvement as well.

Keywords: ESD, SPICE, macro model, snapback, junction partition

1 INTRODUCTION

Time-to-market and cost-to-market are increasingly important in semiconductor integrated circuit manufacturing. Electrostatic Discharge (ESD) failure is one of the major factors resulting in significant costs and time delay in new product development. This is mainly due to the fact that trial-and-error approaches currently still dominates on-chip ESD protection designs.

Predicting the ESD performance of a design prior to manufacturing, just like in regular circuit design, is very appealing. SPICE-type circuit simulation of ESD events with accurate compact models can help reduce design iterations and cost. The simulation provides useful insight on the interaction between ESD and core function circuits and helps ensure that both ESD protection and core circuitry work properly.

Describing the device operation in the ESD voltage/current space through compact models is one of the most critical challenges for ESD circuit simulations. Fig. 1 shows a typical ESD protection scheme used in integrated circuits. ESD structures are connected between I/O pins (IN or OUT) and power supply pins (VDD or VSS) for I/O protection and between VDD and VSS pins as power clamps. ESD protection circuitry/devices are designed to be transparent to the core circuit. They are typically in the off-state under normal operating conditions. They turn-on and provide a low impedance path to Ground in order to dissipate the spurious static charge resulting from an ESD event. MOS devices operating in snapback mode are widely used for ESD protection. A positive ESD stress applied to the drain of the MOS device raises its voltage to a level, *Vt1,* which causes the device to 'snapback' to a lower voltage, *VH*, subsequently creating a low impedance shunting path. Under a negative ESD stress, the forward biased MOS backgate/Drain diode provides such a low impedance path.

Devices under ESD stress operate at currents and voltages that are well beyond the intended operation of the typical devices in a submicron CMOS process technology. Standard SPICE models do not describe high current characteristics and do not address many of the physical phenomena, such as 'snapback' in MOS transistors, particular to the ESD events. Consequently Standard SPICE models cannot predict device behavior under ESD stress conditions.

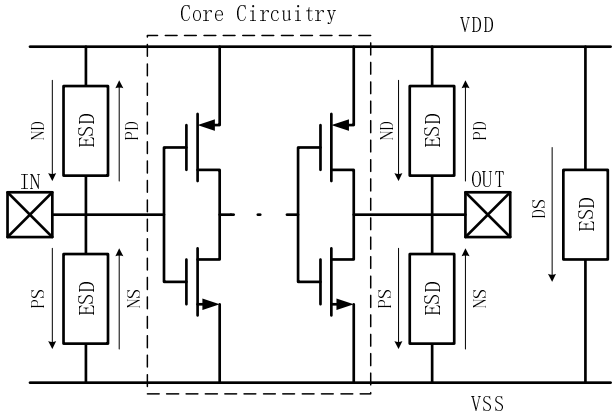

Fig. 1: Typical ESD protection scheme.

ESD simulation using compact models that describe snapback phenomenon in MOS devices has been reported by several groups [1-6]. The models have achieved success in describing the snapback behavior of MOS devices. Among them, the device model originally developed in [5] provides a practical approach in which all major physical effects for snapback phenomenon are intrinsically included and can be used to accurately simulate the high current and high voltage characteristics under an ESD event. However, device characteristic under a negative ESD stress has not been addressed at all or not enough in those models, which may lead to incorrect results in circuit simulation.

In this paper, the device model that has been developed to accurately simulate snapback behavior of MOS devices is to be reviewed. Subsequently Source/Drain junction partition in MOS snapback modeling will be investigated

and a new enhancement on snapback modeling based on the partition will be presented.

2 SNAPBACK MODELING

2.1 Snapback in MOS

Snapback in a MOS device is due to the turn on of the parasitic lateral bipolar transistor (BJT) composed of the Drain/Body/Source of the MOS transistor. The BJT is triggered by the substrate current *Isub*. When the drain voltage *Vds* reaches the snapback trigger voltage *Vt1*, *Isub* becomes high enough to cause a voltage drop across the substrate resistance (*Vbe* for the BJT) that turns on the parasitic BJT. Consequently, *Vds* drops and remains at a lower holding voltage. The device behavior is determined by the MOSFET before snapback and the parasitic BJT dominates after snapback.

The substrate current results mainly from impact ionization in the Drain/Body junction of the MOS (or the avalanche in the Base/Collector junction). It is a function of *Vds* and the gate voltage *Vgs* before snapback and is independent of *Vgs* after snapback.

Besides the avalanche current, gate induced drain leakage (GIDL) also contributes to the MOS substrate current. GIDL is caused by band to band tunneling in the drain region underneath the gate and can be the dominant component when *Vgs*=0 in advanced technologies.

The displacement current, defined as the rate at which the charge is dissipated in the drain (i.e. *dV/dt),* also plays a significant role. Another important transient phenomenon is the finite time required for the BJT to turn on. It is often the limiting factor for the turn on speed of ESD protection circuit which is very important for protection performance.

2.2 Basic Snapback Models

A MOS compact model for ESD simulation is an extension of the standard MOS model with three additional components: a BJT, a current source and a resistor (Fig. 2). The BJT is for the parasitic bipolar transistor and is typically modeled by Ebers-Moll (EM) or Gummel-Poon (GP) equations.

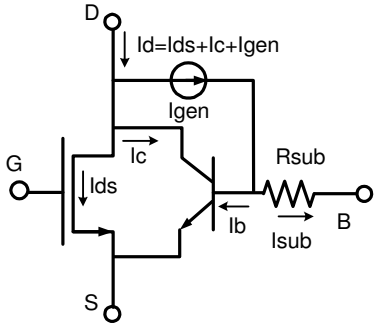

Fig. 2: A typical snapback MOS model

The current source is for the substrate current. Its main contributor is the avalanche current which is given by

$$Igen=(M-1)\cdot(Ids+Ic) \tag{1}$$

or

$$Igen=(M_{MOS}-1)\cdot Ids+(M_{BJT}-1)\cdot I_C \tag{2}$$

to account for the independence of the current from the gate voltage after snapback [3]. *Ids* is the MOS surface drain current, and *Ic* is the BJT collector current. *M, M_{MOS}* and *M_{BJT}* are for the multiplication factor, which is described by the "Miller formula" [7]. In compact models, *M* is often implemented in exponential form:

$$M = \exp\left[k1(Vd - Vdsat - d1)\right] + \exp\left[k2(Vd - Vdsat - d2)\right] \tag{3}$$

where *k1, k2, d1* and *d2* are fitting parameters.

The model implementation includes several different approaches, namely dedicated circuit simulator models, behavior languages such as Verilog-A, and subcircuits containing complicated voltage controlled current sources, either as a behavioral language module or as a SPICE component. Each implementation method has its limitations attributed mostly to the complexity of the explicit current source.

2.3 Macromodel using Standard Devices

A macro model, shown in Fig. 3, that uses advanced industry standard models, eliminates the need to derive a custom model as in [1-4]. In this new approach the explicit current source is removed since all key effects in MOS snapback modeling are intrinsically included in the MOS and BJT compact models. The avalanche and GIDL currents are built in the MOS and BJT models. The displacement current or *dV/dt* effect is modeled by the Collector/Base junction capacitance in the BJT. The transit time of the BJT and separate *M* for the MOS and the BJT are also included.

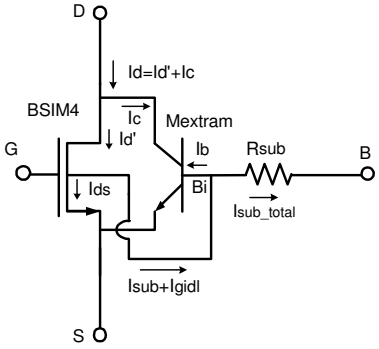

Fig. 3: A new snapback macro model

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3 MODEL WITH S/D JUNCTION PARTITION

3.1 Model Discrepancies

The macro model shown in Fig. 3 describes the snapback behavior of MOS devices very well. However, it fails to model accurately the impedance for negative *Vds*. To model snapback correctly for a typical ESD NMOS protection device, the resistance value of the substrate resistor in the equivalent circuit shown in Fig. 2 and Fig. 3 must be in the range of several hundred Ohms. But the typical resistance of the Drain/Body diode is only a few Ohms when it is measured with the junction forward biased.

On the other hand, we have also found discrepancy in the value of the Base/Collector junction capacitance. The capacitance has significant impact on trigger voltage *Vt1* due to the effect of *dV/dt* [8]. The capacitance value obtained from the dependence of *Vt1* on pulse rise time is smaller than the value directly measured from the whole Drain/Body junction.

Snapback holding voltage *VH* depends on various factors. The current gain (beta) of the BJT is the most significant. It has been found that the beta extracted from a Gummel plot needs to be adjusted higher to fit the measured *VH*. This means that the base current of the BJT for correct *VH* modeling needs to be smaller than the measured current from the substrate terminal. Moreover, the base current also indicates much higher resistance in simulation than in measurement.

It is believed that only a portion of the Drain/Body and Source/Body junctions contribute to the parasitic BJT [1]. This could be the direct cause of the above discrepancies.

3.2 Enhanced Model with Junction Partition

To account for their partial contribution to the parasitic BJT, the Drain/Body and the Source/Body junctions need to be partitioned in the model [6]. Two diodes are added to the equivalent circuit in Fig. 3 to implement the partition (Fig.4). The new macro model for NMOS has five basic components: a MOS transistor for the main device, a three terminal parasitic BJT transistor, a resistor for the substrate resistance, and two diodes. The MOS is modeled by BSIM4 and the BJT by a proprietary bipolar model that is very similar to Mextram.

In a typical ESD protection configuration the Body and Source terminals are shorted together. Therefore, when *Vds* is greater than zero, the impact of the two diodes is negligible. When *Vds* is negative, the diode between the drain and the substrate terminals becomes dominant.

The total substrate current for snapback modeling, which is equivalent to *Igen* in Fig. 2, in the new equivalent circuit is

$$Igen = Isub + Igidl + Iavl + Idio1 \quad (4)$$

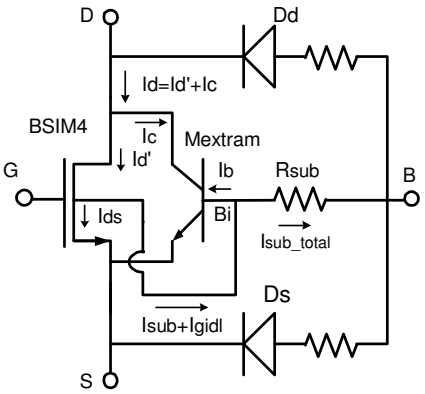

Fig. 4: Macro model with Drain\Source junction partition.

Isub is the impact ionization part of the substrate current in the MOS component, which is an exponential function of (*Vds-Vdseff*) and depends on *Vgs* and *Leff*. The GIDL current *Igidl* depends on *Vds*, *Vgs* and *Vbs*. BSIM4 expresses it as an exponential function of (*Vds-Vgs*) [9].

The avalanche current of the Collector/Base junction in advanced BJT models (*Iave*) is also an exponential function that depends on the voltage drop over the junction [10]. *Iave* is independent of the MOS gate voltage *Vgs*.

Idio1 is the current through the diode Dd. When *Vds*>0 it is negligible and *Igen* is basically the same as the one without the diodes. When *Vds*<0, *Idio1* dominates total *Ids* current.

When the device is measured in a forward Gummel configuration, the total body terminal current or the base current is

$$Ib = Ib' + Idio2 \quad (4)$$

where *Ib'* is the base current from the BJT and *Idio2* is from the forward biased Source/Body diode Ds.

4 SIMULATION AND DISCUSSION

The simulation data for the model has been correlated with measurement data. The MOS model and the BJT model were first extracted from IV curves in normal operating region using standard model extraction methodology. Then the substrate resistance R_{sub}, the collector capacitance CJC and the current gain BF in the BJT model were determined from the snapback characteristics. In the final step, the parameters in the diodes for junction partition were obtained from the IV curve for Vds<0 and the total drain junction capacitance.

The snapback were measured using transmission line pulse (TLP) technique with a Barth Model 4002 TLP tester. The TLP pulse width used was 100ns and the rise time was varied between 200ps, 2ns and 10ns. Transient simulations were carried out using voltage pulse sequences as the input. The *Va* and *Ia* values in snapback curves were extracted from the region of I, V pulse waveforms where the current and voltage were stable.

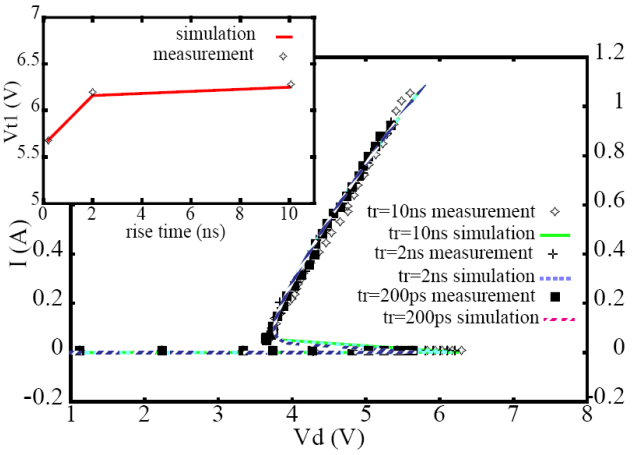

Fig. 5: Snapback curves of a ggNMOS device for different rise times (tr=200ps, 2ns, 10ns)

Fig. 5 depicts a comparison of simulation and TLP measured data of a ggNMOS device for different rise times. *Vt1* values are plotted as a function of the pulse rise time in the inserted plot. When t_{rise} decreases to 200ps *Vt1* reduces by approximately 0.6V from the t_{rise}=10ns value due to the increase of displacement current. The capacitance value from the BJT model that fits the data is lower than the measured value. The ratio for the device in Fig.5 is about 0.9.

Fig. 6 shows a comparison of simulation and quasi-static TLP measured data of a ggNMOS device. The simulation results show very good agreement with the data for both positive and negative Vds. The resistance in the range of Vds<0 is about 5 Ohm, compared with the Rsub value of about 800 Ohm.

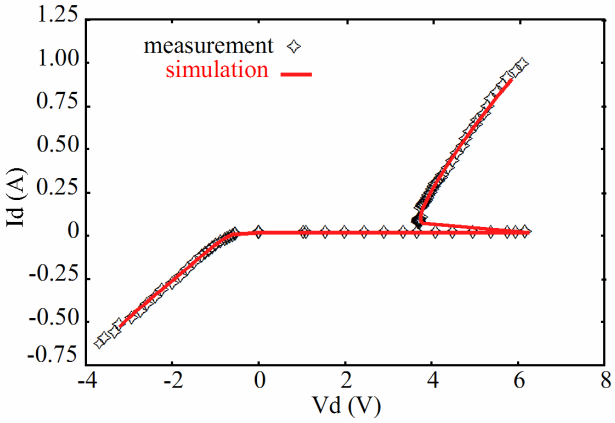

Fig. 6: Comparison of simulation and measurement data of a ggNMOS device.

Fig. 5 depicts simulation and measurement data corresponding to equation (4). It shows that after junction partition the model fits the base current curve of the parasitic bipolar much better.

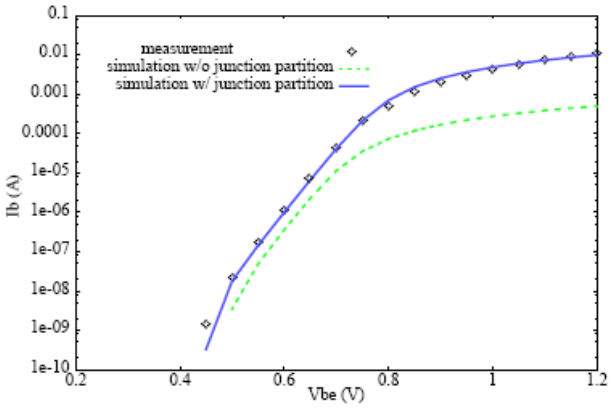

Fig. 7: Base current comparison with and without Drain and Source junction partition.

5 CONCLUSION

Partition of the Drain and Source junctions in MOS snapback model has been discussed using a new macro model approach. The model is based on industry standard models only and intrinsically includes all major physical effects particular to snapback. The partition enhances the MOS snapback model and makes the model valid for both positive and negative drain voltage stresses. The comparison of simulation and measured data of a Grounded-Gate NMOS shows good agreement. The total drain capacitance and the base current curve of the parasitic bipolar shows significant improvement as well.

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