Quantum Transport Simulation of Si FinFET: Approaching Optimal Characteristics for 10 nm High Performance Devices

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ABSTRACT

We utilize fully self-consistent quantum mechanical simulator based on Contact Block Reduction (CBR) method [1] to optimize 10 nm FinFET device to meet ITRS requirements for High Performance (HP) Double-Gate (DG) devices. Fin width, gate oxide thickness, and doping profile are chosen to reflect realistic values and to boost on-current while keeping the total leakage within reasonable limits. We find that the device on-current approaching the value projected by ITRS for HP devices can be obtained using conventional (Si) channel. Our simulation results also show that quantum nature of transport in ultra small devices significantly enhances the intrinsic switching speed of the device. Small signal analysis has been performed to extract device capacitances. Sensitivity of device performance to the process variation at room temperature has been investigated.

Keywords: FinFET, process variation, CBR, switching speed, cut-off frequency.

1 INTRODUCTION

Industry trends in conjunction with Moor's law [2] has led to the creation of so-called 'roadmaps' [3] for CMOS technology, which suggests that conventional bulk MOSFETs are approaching some fundamental physical limits in the not too distant future [4]. DG MOSFETs, particularly quasi-planer FinFET [5] – a promising candidate due to its robustness to short channel effects, emerged to continue scaling down to few tens of nanometer regime. In this work we use fully self-consistent quantum mechanical simulator based on CBR approach [1], [6] to optimize the device geometry and doping profile of a 10 nm FinFET device to meet the performance matrices defined by ITRS [3]. In addition, we investigate rigorously the effects of gate leakage and process variation on the performance of the optimized device structures at room temperature ($27°C$). Figure 1 depicts the geometry of the 10 nm DG FinFET device being investigated in this study. Fin thickness, t_{Si} of 4 nm and gate oxide thickness, t_{ox} of 1 nm have been used in the simulation. Source, drain and gate doping of 1×10^{20} cm^{-3} with a lightly doped body and a doping gradient (g_{dop}) of $2\ nm/dec$ across source-body and body-drain junctions have been adopted. In this work, effects of top gate on transport have been assumed to be negligible. We also assume the gate work function adjustment of 0.35 eV.

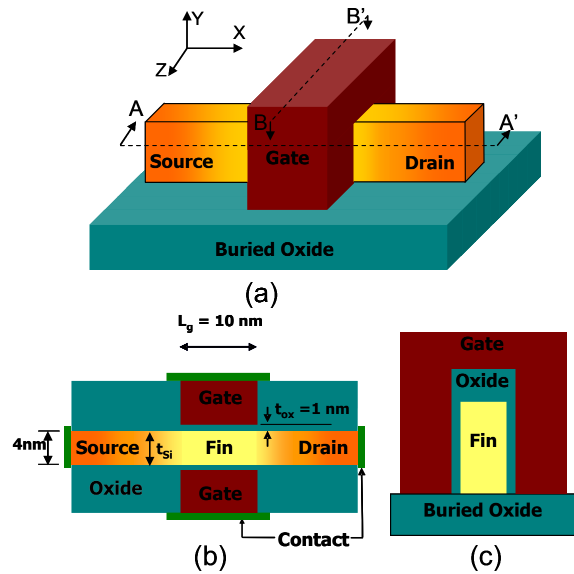

Figure 1: (a) 3D schematic view, (b) top view along A-A′ cross section, and (c) side view along B-B′ cross section.

2 OPTIMIZATION AND SIMULATION RESULTS

Optimization of a device depends on its specific application. In this work we concentrate on 10 nm DG HP technology logic devices [3]. Regarding efficient design of a FET L/Λ_1 [7] is a fundamental measure of the quality of the FET, where Λ_1 is the scale length and $L/\Lambda_1 \gg 1$ is desired. For small value of L/Λ_1 different 2-D effects such as DIBL, high output conductance and threshold voltage, V_T roll-off becomes noticeable [8]. For DG devices the minimum gate length L_{min} (nominal design) can be estimated as $L_{min} \sim 1.5t_{Si} + 9t_{ox}$ assuming SiO_2 gate dielectric and $L/\Lambda_1 = 1.5$ [9], which necessitates t_{Si} on the order of 3 nm

and t_{ox} on the order of 6 Å for $L_{\min} = 10\ nm$. For narrow fin width devices t_{Si} plays the dominant role to control device performance [10]. However, in this work we chose t_{ox} = 10 Å to reflect a more realistic value, as manufacturability of SiO_2 of 6 Å thickness is still not known [3]. For HP devices the major requirement is higher value of on-current, I_{ON} (I_D at $V_{DS} = V_{GS} = V_{DD}$) keeping the off-current, $I_{off} = I_{sd,leak} + I_G$ at an acceptable level, where $I_{sd,leak}$ (I_D at $V_{GS} = 0\text{V}, V_{DS} = V_{DD}$) is the subthreshold source-drain leakage current, and I_G is the total gate leakage current. Again, I_{off} is determined by both V_T (determined by t_{Si} with $t_{Si} \ll L_g$) and subthreshold swing, S according to $I_{off} \propto 10^{-(V_T/S)}$ [9]. Therefore, the requirement of high drive-current (smaller V_T) results in significantly higher value of $I_{sd,leak}$ (particularly with high source/drain doping) as t_{Si} increases for the same gate work-function adjustment, which is evident from Figure 2.

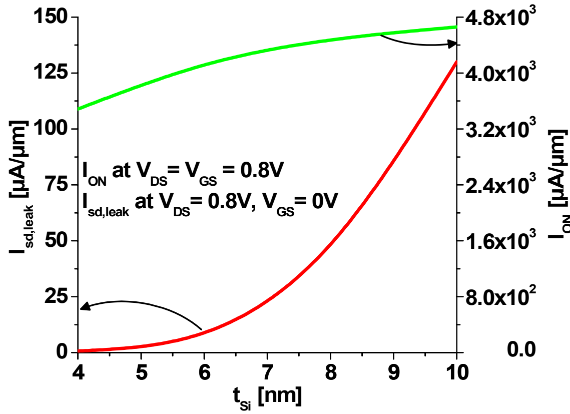

Figure 2: I_{ON} and $I_{sd,leak}$ as a function of t_{Si}.

A fully volume inverted channel (both at saturation and subthreshold regime of operation) across the entire channel, which improves the turn-off behavior significantly, can be obtained when $t_{Si} \le L_g/2$ for 10 nm devices as observed in our simulation. However, decreasing t_{Si} below 5 nm results in a rapid growth in the uncertainty of threshold voltage variation due to quantization effects [8]. Also as t_{Si} becomes thinner, it becomes difficult to maintain uniformity in thickness. To compensate the degradation in I_{ON} due to thinner t_{Si}, smaller value of g_{dop} can be adopted, which on the other hand increases $I_{sd,leak}$, as can be seen from Figure 3. Note that $I_{sd,leak}$ is more sensitive to t_{Si} than to g_{dop}. Even though higher value of g_{dop} yields smaller value of I_{off} and S, for HP devices smaller value g_{dop} is desirable due to the requirements of higher value of I_{ON}. Step doping would yield the highest I_{ON}, but in reality even $g_{dop} = 1\ nm/dec$ is challenging to achieve [11]. Table 1 summarizes the performances matrices as projected by ITRS for 10 nm HP DG devices with $V_{DD} = 0.8$ V along with the simulation results obtained in this work.

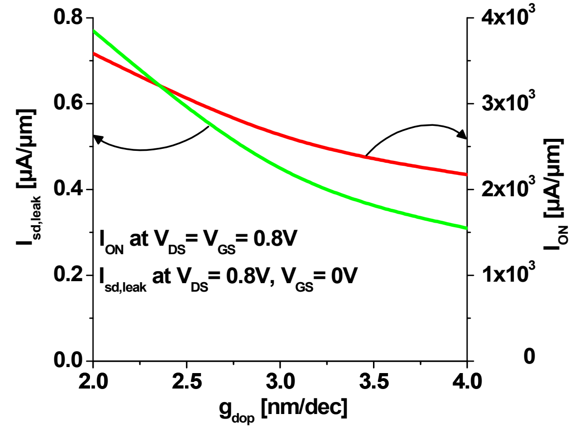

Figure 3: I_{ON} and $I_{sd,leak}$ as a function of g_{dop}.

2.1 Gate oxide and equivalent oxide due to quantum confinement in gate/channel

Equivalent oxide thickness is defined by ITRS [3] as $EOT = T_d/(\kappa/3.9)$, where T_d and κ are the physical thickness and permittivity of the dielectric respectively. In our case $EOT = t_{ox}$, since we use SiO_2 as gate dielectric. $t_{inv_poly} = t_{inv} + t_{poly}$ is defined by ITRS as an equivalent oxide thickness in series with t_{ox} introduced by poly depletion in gate, t_{poly} and charge set back from SiO_2/Si interface, t_{inv} due to quantum mechanical confinement in the channel. Note that $EOT_{elec} = EOT + t_{inv_poly}$. Due to the use of highly doped gate in our simulation, the effect of poly depletion is negligible [12] . We find from the simulations that t_{poly} is mainly due to quantum mechanical confinement of carriers in the gate and is comparable to t_{inv}. The ratio of EOT/EOT_{elec} calculated using ITRS projected values [3] is 0.6 whereas in our case it is 0.57.

2.2 On-current, subthreshold source-drain leakage and gate leakage current

The maximum possible gate leakage current density $J_{g,limit}$ (calculated at $V_{GS} = V_{DD}, V_{DS} = 0\text{V}$) for 10 nm DG HP devices as projected by ITRS is 2200 A/cm^2, considering contribution from both gates. The corresponding value obtained from our simulation is 5667 A/cm^2 with SiO_2 as gate dielectric. The resulting 2.5 times higher value of the

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leakage current can be cured by using a high-k dielectric with the same EOT.

Parameter	ITRS	Simulation
EOT [Å]	6	10
t_{inv_poly} [Å]	4	7.5
EOT_{elec} [Å]	10	17.5
$J_{g,limit}$ [A/cm^2]	2200	5667
$V_{t,sat}$ [mV]	192	140
$I_{sd,leak}$ [μA/μm]	0.22	0.75
I_{ON} [μA/μm]	4550	3584
$C_{g,ideal}$ [F/μm], per gate	3.46E-16	1.97E-16
$C_{g,total}$ [F/μm], per gate	5.25E-16	2.76E-16
τ [ps]	0.18	0.12
$1/\tau$ [GHz]	5556	8333

Table 1: ITRS projection vs. simulation (ballistic) result.

GIDL current is negligible due to the use of source/drain-gate underlap [13]. $I_{sd,leak}$ and I_{ON} as projected by ITRS [3] for 10 nm HP DG devices are 0.22 $\mu A/\mu m$ and 4550 $\mu A/\mu m$ respectively, whereas the corresponding values obtained in this work are 0.75 $\mu A/\mu m$ and 3584 $\mu A/\mu m$. Figure 4 shows the transfer characteristics for the considered device at $V_{DS} = 0.8\,\text{V}$ and $0.1\,\text{V}$. Subthrshold slope, S of 75 $m\text{V}/dec$ (at $V_{DS} = 0.8\,\text{V}$), DIBL of 43 $m\text{V}/\text{V}$ and saturation threshold voltage $V_{t,sat}$ of 140 $m\text{V}$ has been obtained for the considered device. The value of $V_{t,sat}$ as projected by ITRS is 192 $m\text{V}$.

2.3 Intrinsic delay and cut-off frequency

The intrinsic propagation delay, τ, is defined by ITRS as the propagation delay through a single device driving a load of another single device of the same type, and can be expressed as $\tau = (C_{g,tot} \times V_{DD})/I_{ON}$, where $C_{g,tot}$ is the total capacitance of the load device at $V_{GS} = V_{DD}, V_{DS} = 0\text{V}$. To calculate τ the maximum value of $C_{g,tot}$ must be used in order to get the worst case propagation delay. The total capacitance $C_{g,tot}$ is the sum of $C_{g,ideal} = [\varepsilon_{ox}/(EOT_{elec})] \times L_g$ and parasitic capacitances, C_p. Figure 5 shows the 1D distribution of capacitance along the channel. Note that in our simulator all the capacitances are calculated using the exact formula $\partial Q/\partial V$ and we use analytical formula as described above to compare with ITRS [3] values. It is evident from Figure 5 that fringe capacitance on each side of

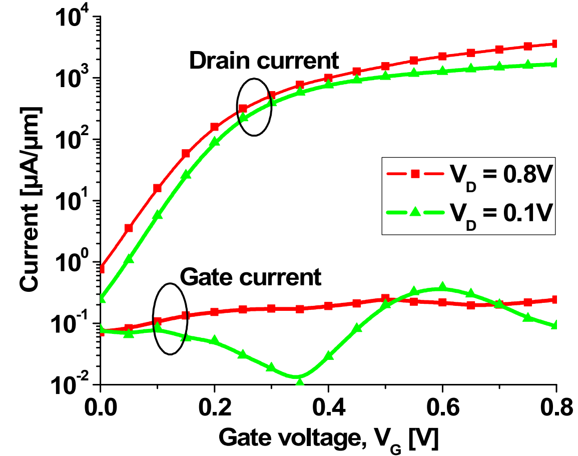

Figure 4: Transfer characteristics at $V_{DS} = 0.8\text{V}$ and 0.1V.

the gate is not negligible and therefore, must be taken into account while calculating the intrinsic delay, τ. As projected by ITRS, C_p is 52% of $C_{g,ideal}$, whereas in this work it is 42%. Note that the dip in capacitance curve at high gate voltage is due to fact that the potential in the vicinity of the center of the fin tends to saturate at high gate voltage [14] and therefore, does not respond to small signal perturbation. The value of τ as obtained from our simulation is 0.12 ps while the corresponding value projected by ITRS is 0.18 ps.

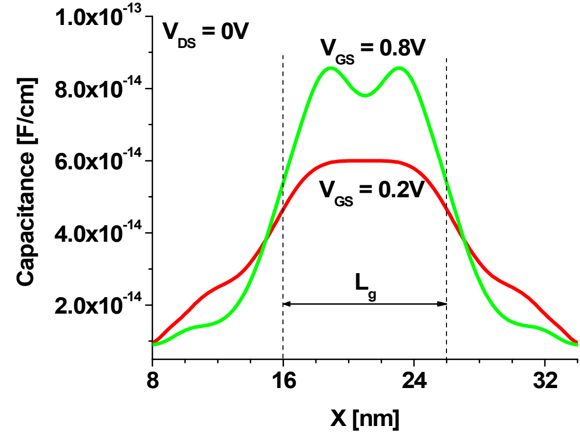

Figure 5: 1D distribution of capacitance along the channel.

We also assess the RF performance of the device by extracting the cut-off frequency, f_T, which is a measure of the maximum useful frequency when the FinFET is used as an amplifier. The cut-off frequency is the frequency at which the short circuit current gain of a single transistor becomes unity and can be calculated using $f_T = (1/2\pi) \times (g_m/C_{g,tot})\big|_{V_D = V_{DD}}$, where g_m and $C_{g,tot}$ are the transconductance and total capacitance of the device respectively and both evaluated at $V_{DS} = V_{GS} = V_{DD}$. The

value of f_T obtained from our simulation is 4528 GHz with $C_{g,tot} = 2.34\, pF/cm$ and $g_m = 6.66\ mS/\mu m$.

3 PROCESS VARIATION

We investigate performance degradation due to process variation in t_{Si} (by $\pm 10\%$), t_{ox} (by $\pm 20\%$), g_{dop} (by $\pm 10\%$) and L_g (by $\pm 12\%$) at $T = 27°C$. Considering the variations in t_{Si} and t_{ox}, the degradation in I_{ON} is less than 4% for our FinFET. However, $I_{sd,leak}$ is found to be sensitive to changes in t_{Si} and t_{ox}, particularly to t_{Si}. For a 10% increase in t_{Si}, $I_{sd,leak}$ increases by 77% from its nominal value of 0.75 $\mu A/\mu m$, whereas even for a 20% increase in t_{ox}, corresponding increases is still smaller, 53%. The worst case degradation in device performance is found for a combination of $t_{Si} = 4.4\ nm$ and $t_{ox} = 1.2\ nm$ for which $I_{sd,leak} = 2.06\, \mu A/\mu m$, $S = 84\ \text{mV}/dec$ and $DIBL = 62$ $m\text{V}/\text{V}$ have been obtained.

The major limiting issue to optimize device performance in nanometer regime is the excessive gate leakage due to the requirement of thinner gate oxide to control SCEs. The acceptable tolerance window for variation in t_{ox} is very narrow as found in our simulation unless the dielectric is changed. For a 20% decrease in t_{ox}, keeping other device dimensions constant results in a significant increase of I_G from 0.24 $\mu A/\mu m$ to 1.91 $\mu A/\mu m$.

Considering variation in L_g and its relative position with respect to source/drain, highest degradation in I_{ON} $(\sim 14\%)$ has been found for a 10% reduction in L_g, when this reduction is introduced at the source end keeping the end point of gate on the drain side fixed. For this case, $I_{sd,leak}$ is also found to be $1.20\, \mu A/\mu m$, significantly higher than the nominal value of $0.75\, \mu A/\mu m$.

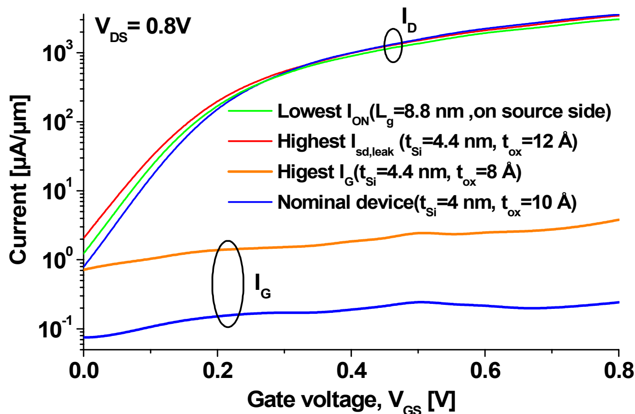

Figure 6: Transfer characteristics due to process variation.

For an increase in g_{dop} by 10% on each or both sides of the gate, both I_{ON} and $I_{sd,leak}$ are found to be insensitive. Figure 6 shows the transfer characteristics due to process variations showing lowest value of I_{ON}, highest value of $I_{sd,leak}$ and highest value of I_G at $V_{DS} = 0.8\text{V}$.

4 CONCLUSION

Using the fully self-consistent CBR quantum transport simulator, we have analyzed the performance and process variation of an optimized 10 nm FinFET device with conventional Si 4 nm thick channel and realistic doping gradient (2 nm/dec) and gate oxide thickness (1 nm). We find that due to quasi-ballistic nature of the transport in this ultra-scaled FinFET device, the value of on-current is indeed approaching the value projected by ITRS for 10 nm DG HP devices. At the same time, the strong spatial quantization effects lead to the significant improvement of the intrinsic propagation delay τ (up to 0.12 ps), due to the effective capacitance reduction. The other major device characteristics are found to be close to the ITRS requirements meaning that performance matrices for 10 nm DG HP devices as projected by ITRS are achievable with Si FinFETs.

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