Single Walled Carbon Nanotubes based Three Dimensional Flexible Electronics

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ABSTRACT

Single Walled Carbon Nanotubes (SWNTs) with their superior electrical and mechanical properties are very strong candidates for future electronic applications. CMOS electronics are constantly being scaled down to accommodate more devices. Alternative device geometries are being investigated, as scaling of devices cannot be maintained by reducing the geometry alone due to the limitations in gate length and oxide thickness. Alternative device geometries facilitate further miniaturization of devices while providing new platforms for nanoscale devices. We introduce a room temperature route for integrating SWNTs on flexible substrates. Flexible electronics is an emerging area of research. Coupled with this area, nanoscale devices especially in 3D would allow high density miniaturization of future micro and nanoelectromechanical systems as well as 3D microelectronics. 3D structures are micromachined on top of a parylene-C substrate**.** SWNTs are then assembled using dielectrophoresis between top and the bottom metal electrodes, providing a one step method to make 3D SWNT based devices directly on flexible substrate. Electrical measurements of the device demonstrate a linear behavior with a resistance of 900 Ω. This approach is compatible with conventional semiconductor processing and hence will find extensive applications in 3D nanoelectronics, NEMS and nanosensors.

Keywords: SWNT, flexible, 3D, electronics, Parylene, nanotube

1 INTRODUCTION

CMOS electronics are constantly being scaled down to accommodate more devices. Alternative device geometries and materials are being investigated, as scaling of devices cannot be maintained by reducing the geometry alone, due to the limitations in gate length and oxide thickness. Alternative device geometries facilitate further miniaturization of devices while providing new platforms for nanoscale devices. In the materials regime Single Walled Carbon Nanotubes (SWNTs) with their superior electrical, mechanical and thermal properties are very strong candidates for future electronic applications[1].

Currently the only technology that is available for the integration of nanotubes into three dimensional architectures is to grow them vertically using chemical vapor deposition (CVD). The CVD based nanotube growth process is a high temperature process (>500°C) that uses pre-patterned catalysts deposited either on a buried electrode[2,3] or directly on metal electrodes[4]. Also CVD grown SWNTs have a high number of semiconducting[5] SWNTs, which might pose potential problems for use in applications such as interconnects. Further the high temperature requirements of the CVD process restrict fabrication of SWNT based devices on flexible substrates directly. Hence the only methods that have been reported on SWNT based 3D devices on flexible substrates is by transferring[6] them to polymer substrates. Flexible electronics represents a whole new form of electronics built on flexible plastic substrates that would open applications in flat panel displays[7,8], flexible nanoelectronics[9], switches[10], low cost sensors, and other disposable electronic devices.

In this paper, for the first we introduce a room temperature route for integrating SWNTs on flexible substrates. A top-down micro-fabrication technique is used to make the 3D platform which facilitates the room temperature bottom-up assembly of SWNTs using dielectrophoresis.

2 EXPERIMENTAL PROCEDURE

2.1 Fabrication

The fabrication and assembly process is illustrated in Fig. 2. The fabrication of the 3D micromachined platform begins with the deposition of a 10 µm thick Parylene-C at room temperature on a 3” silicon wafer. Ths is followed by the deposition and patterning of the first metal layer (Cr/Au - 175A/1500A) using a lift-off process. A 0.7µm thick

conformal parylene-C dielectric layer is then deposited on top of the silicon wafer. The second metal layer (200Å/1500Å) is then deposited and patterned using the same liftoff technique used for the first metal layer.

The inter dielectric parylene layer is then etched using oxygen plasma in a reactive ion etcher (RIE) with the second metal layer as a mask. The two metal layers serve as the electrodes for the 3D dielectrophoretic assembly of the SWNTs. Once the 3D platform is ready, the parylene C substrate containing the platform can be peeled off from the silicon wafer for assembly and testing.

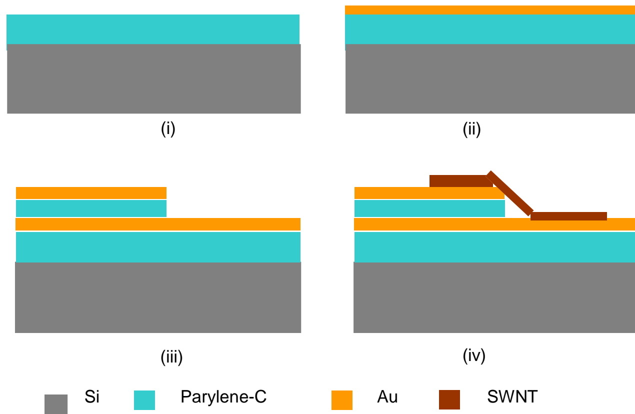

Figure 1: Schematic fabrication and assembly process flow.

2.2 Assembly

Commercially available SWNTs grown by CVD, purified and dispersed in an aqueous solution were used for the dielectrophoretic assembly. The average diameter of the SWNT is between 2-5nm and the average length varied from 3-5 µm. An AC voltage of 5 V peak-to-peak with a frequency of 10MHz is utilized in our assembly. The voltage is turned on and a droplet (2-3µl) of the SWNT solution is dispensed on to the chip containing the microelectrodes. After 30 seconds of assembly, the sample is blow dried with 5 psi nitrogen and the power is turned off resulting in assembled SWNTs bridging the top and the bottomn electrodes. The resulting assembly is first confirmed by continuity measurements and then imaged using scanning electron microscope.

3 RESULTS AND DISCUSSION

The assembly of the SWNTs is shown in figure 2. Figure 2A shows the flexible substrate with the 3D platforms fabricated on it. Figure 2B is a closer optical image of one of the 3D platforms. The assembled SWNTs after dielectrophoresis is shown in figure 2D. Well aligned parallel arrays of SWNTs are assembled between the top and the bottom electrode.

Cross sectional image of all the assembled SWNTs show that the SWNTs assembke at a particular angle to the surface.The angle at which the SWNTs attach to the substrate depends on various factors including the length of

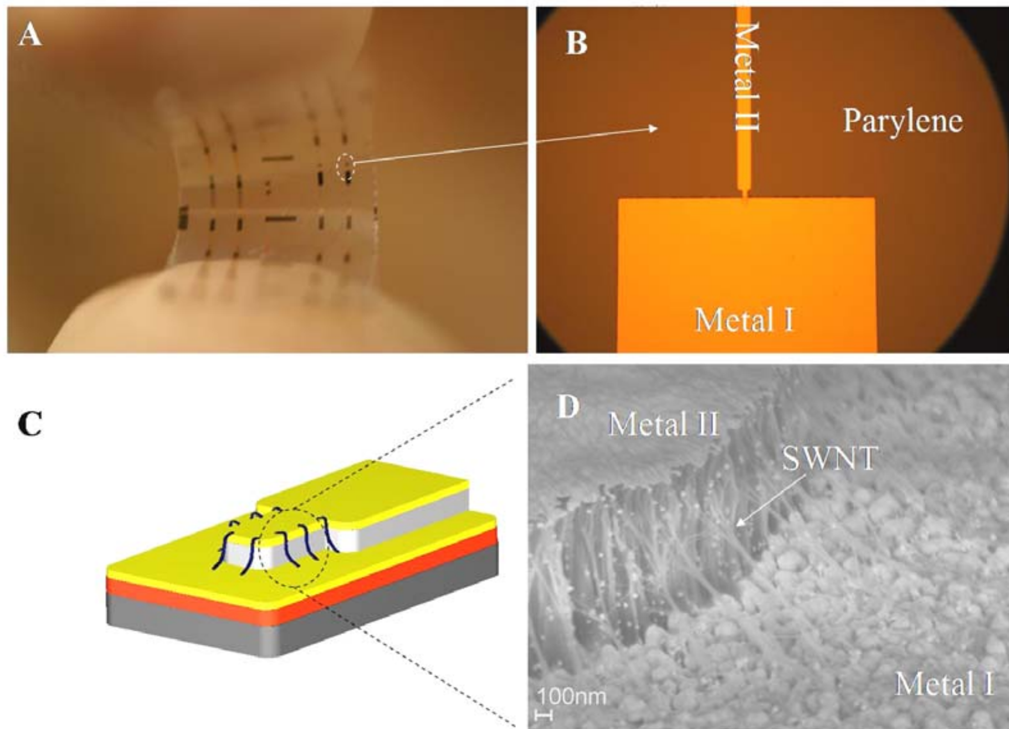

Figure 2: (A) Picture of the micromachined platform on flexible substrate. (B) Optical micrograph of the 3D platform. (C) Schematic of the 3D platform. (D) High resolution SEM image of the assembled SWNTs connecting the top and bottom electrode.

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CNTs, the thickness of the parylene-C layer and the direction of field lines of the electric field. It is a well known phenomenon that the SWNTs align along the electric field lines and move towards the higher electric field gradient. We believe the most important driving force for this angle is the electric field along with some influence from capillary forces.

Electrical Measurements were carried out on the assembled SWNTs before and after flexing the parylene substrate. The I-V measurement of the assembled SWNTs demonstrated a linear behavior with a resistance value of 900 Ω. This resistance was repeatable even after the substrate was flexed a couple of times. Even though this measured resistance value using our 3D assembly platform is lower than most of the resistance values from SWNTs (100- 200 kΩ) reported[11,12] to date. This resistance value would decrease as SWNT dispersion techniques mature and SWNT-metal contacts are improved.

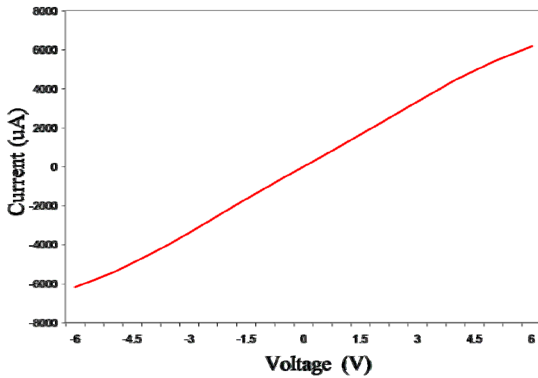

Figure 3: Electrical measurement showing IV characteristics of the SWNT 3D assembly.

4 CONCLUSION

In conclusion, we have developed a powerful room temperature technique that utilizes top-down photolithography and bottom-up dielectrophoresis to manufacture a universal platform for SWNT 3D architectures on flexible substrates. These are the very first reported results in the controlled fabrication of complex 3D geometries of SWNTs on flexible substrates. This technique provides a versatile, low cost and scalable platform for making 3D nanotube/nanowire architecture, which should find immediate and immense implications in the development of nanoelectronic and nano-electromechanical devices for diverse applications ranging from sensors to displays.

5 ACKNOWLEDGEMENT

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