An Efficient Sectionalized Modeling Approach for Introduction of Distributed Avalanche Effects in Bipolar Circuit Design

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ABSTRACT

A reduction technique for an accurate modeling of complex effects manifested in an avalanche regime of bipolar junction transistors is shown in this paper. Bilinear approximation is utilized to significantly reduce computational cost of a model made for precise consideration of breakdown phenomena. The simplification method is practically implemented on the bases of a vertical bipolar compact model Mextram. Extraction of an additional parameters is studied. The reduction technique is quantitatively compared to the model from which it is derived and the results are presented.

Keywords: bipolar transistor, avalanche breakdown, impact ionization, compact model, model reduction.

1 INTRODUCTION

Modeling of breakdown phenomena is becoming a central problem in today's design of high-speed bipolar circuits. It is especially important for the output stages that should simultaneously provide speed and output signal power. The interplay of the device maximum operating frequency and output power requires complex design trade-offs. To this end, an accurate modeling is essential to fully exploit the potential of the advanced Si and SiGe bipolar technologies, and to allow safe circuit design with bipolar transistors operating above the collector-emitter breakdown voltage at open base, BV_{CE0}.

Carrier impact ionization could change the direction and significantly increase the intensity of a transistor base current leading also to instabilities in the device behavior [1]. Main source of the device instabilities is the current crowding effect caused by a considerable lateral base current in the intrinsic transistor region. It creates nonuniform biasing along the base-collector junction. This effect is best visualized by performing 3-dimensional simulation of a typical bipolar transistor as shown in Figure 1, where different tones refer to different current densities in a vertical current flow.

The designers already posses a profound tool that have a possibility to give a respectable prediction of a device behavior in the avalanche operating regime thanks to the quasi-distributed 3-dimensional transistor model [2]. Unfortunately, although very precise, this model suffers form extremely high complexity and inefficiency. This paper shall give a contribution in an efficient modeling of a multidimensional avalanche effects. The main benefit shall be the model that is not too expensive for circuit simulation but nevertheless preserves the accuracy of a previous models developed for the same purpose. The two models are compared in terms of simplicity and accuracy and verified by measurements on sophisticated test devices.

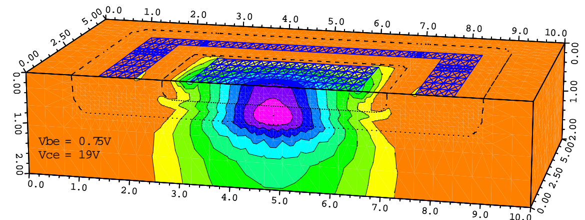

Figure 1: 3-dimensional TCAD simulation of a vertical bipolar transistor in the avalanche breakdown regime.

2 MULTITRANSISTOR MODEL

One way to address multidimensional avalanche effects in circuit design is to employ sectionalized bipolar transistor models. The basic idea is to partition the transistor base under the emitter into vertical sections associating each of them with a separate intrinsic transistor model as it is shown in Figure 2. The bases of the neighboring sections are coupled to each other with an effective variable base resistance being a fraction of the total base resistance. The network of intrinsic transistors is capable of capturing the distributed character of the main transistor current, but its main drawback is the complexity. A circuit representation of the sectionalized intrinsic transistor model is shown in Figure 3, while the extrinsic part remains unmodified.

There have been attempts to decrease this complexity using problem symmetry and sacrificing the model accuracy using rather small number of sections [3]. A novel technique to significantly reduce the computational cost of sectionalized transistor models is proposed in this paper.

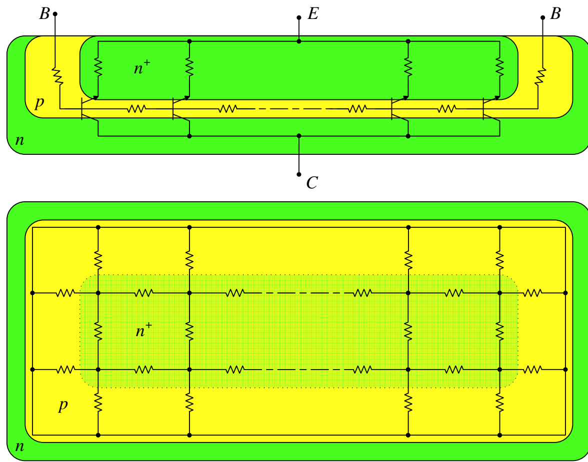

Figure 2: The cross-section side view and the top view of the typical BJT device with the schematics of a sectionalized intrinsic transistor model needed for an accurate prediction of the distributed avalanche effects.

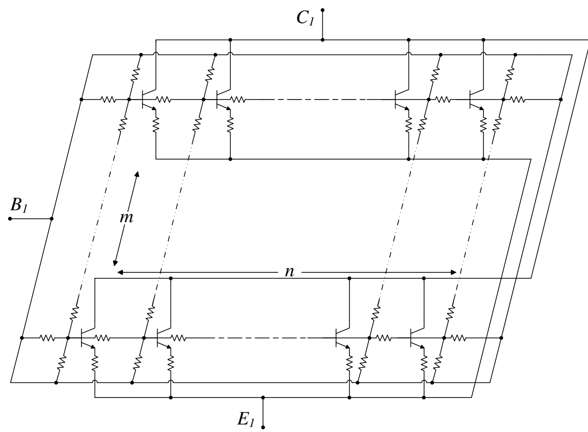

Figure 3: The sectionalized intrinsic transistor model.

2.1 Bilinear Approximation as a Reduction Technique

Firstly, if the emitter possesses a rotational symmetry of order s, that attribute should be utilized to reduce multitransistor model complexity by a factor of s. In practice, since the emitter is often rectangular with even number of base stripes, this will be assumed onwards if not indicated otherwise, the computational time shall be divided by a factor of 4. Furthermore, a proposed method of reduction employs only two one-dimensional chains of full intrinsic transistor sections along the symmetry lines of the emitter contact using bilinear interpolation to get the effect of full transistor matrix. Moreover, only four full intrinsic transistor elements (center one, corner one, one on the horizontal and one on the vertical axis corresponding to the adequate row and column) have been used to interpolate the particular inner transistor current. This is schematically shown in Figure 4. Currents (base, emitter and

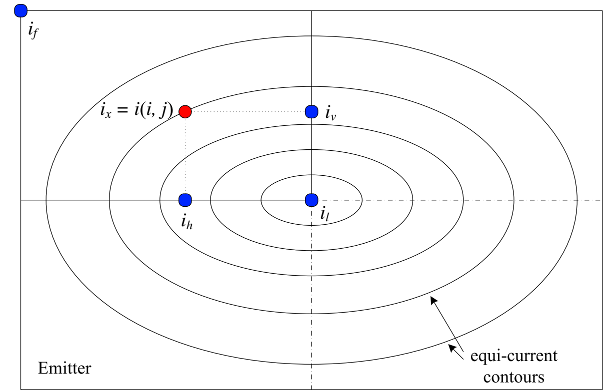

Figure 4: Approximation of the inner transistor segment currents on the basis of four (center, corner, horizontal axis, vertical axis) full intrinsic transistor elements.

collector) of the inner transistor segment in the row i and the column j, $i_x = i(i, j)$ are interpolated using the following expression:

$$i_x = \frac{(i_h - i_f)(i_v - i_f)}{i_l - i_f} + i_f \quad (1)$$

where $i_f = i(1, 1)$ is the corresponding current of the corner full intrinsic transistor element, $i_f = i(m/2, n/2)$ current of the center intrinsic transistor element, $i_h = i(m/2, j)$ current of the corresponding horizontal transistor element, $i_v = i(i, n/2)$ current of the corresponding vertical element and m and n the number of rows and columns of the transistor matrix, respectively. Because the intrinsic transistors model does not have a substrate description, only two currents, for example base and emitter currents, are approximated with the third one, collector current, obtained by a simple addition operation. We can conclude that in the original segmentated model the number of full intrinsic transistor elements would be $m \cdot n$, exploiting symmetry $(mn)/4$, and using proposed reduction method only $(m + n)/2$ with $((m - 1)(n - 1) - 1)/4$ interpolation segments.

2.2 Verilog-AMS Implementation

The original and reduced segmentated models have been practically implemented in Verilog-AMS [4] language. Mextram, vertical bipolar transistor model [5] was used in segmentation process, although HICUM [6], VBIC [7] or some other compact model could be used as well. Intrinsic part of the Mextram, highlighted in Figure 5, is used to create full intrinsic transistor element model that is later multiplied. The extrinsic part

of the Mextram remained the same except for the part between the nodes B_1 and B_2. This part (the resistor and the capacitor) models the internal base distributed resistance under the base-emitter capacitance. Since the model proposed in this work already has a built-in distributed transistor network, incorporation of these two elements would be redundant.

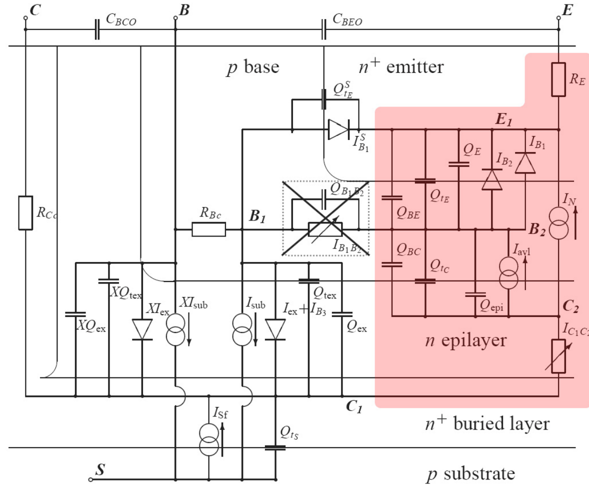

Figure 5: The original Mextram model: Intrinsic transistor (highlighted) and obsolete part (struck-through) when the model with distributed base resistance is used.

The decision on the matrix dimensions, m and n, is on the user. Greater dimensions implicate higher precision, but also as a consequence the problem is more complex and it uses more resources, usually processing time. In the implementation we took assumption of 4-fold rotational symmetry, yet this does not lessen the generality of the method which can even be applied for the multi-finger emitter geometries. Taking into account only one quadrant, the full intrinsic transistor elements are placed on the symmetry lines plus one in the corner while the interpolation transistor segments occupy all other positions in the matrix. The interpolation transistor segment is implemented according to the Equation 1. Schematics of interpolation transistor, composed of two controlled current sources, is given in Figure 6.

2.3 Extraction of Additional Parameter

Beside the standard Mextram parameters, there is only one additional parameter that has to be known in order to fully define the model. The extra parameter is the intrinsic base interconnection resistance, that connects the base nodes of the intrinsic transistor elements and interpolation segments. In practice, to optimize the precision, the model dimensions m and n should be proportional to the emitter length L and width W. When this is the case it yields the interconnection resistance

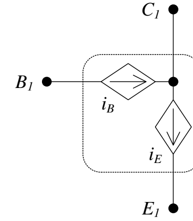

Figure 6: The interpolation Segment: Inner transistor element replacement built of two controlled current sources that represent the base and the emitter current.

R_{bic} extraction formula, which is indeed very similar to the original Mextram estimation expression:

$$R_{bic} = \rho_s \frac{W}{L} \frac{m}{n} \tag{2}$$

where ρ_s is the pinched sheet resistance of the base. Since the R_{bic} models the resistance of equidistant and relatively uniform layers of the intrinsic base, all resistances in the network have the same value.

3 RESULTS

In practice, excellent matches between measured and simulated data are obtained when the number of segments is larger than one thousand. Figure 7 shows the non-uniform normalized base potential distribution that causes current pinch-in. The simulation is performed on a square emitter geometry using a matrix with dimensions 32×32, model with 1024 segments. When symmetry is taken into account, model with only 256 segments remains. Now, the reduced model formulation employs only 32 full intrinsic transistor elements and 224 interpolation segments.

Maximum relative approximation error is in the order of magnitude of 0.1 percent. This relative error for approximated (in this case base and emitter) currents is drawn in Figure 8 as a function of applied DC voltage. Onset of impact ionization occurs around 12V followed by the weak and strong avalanche breakdown.

Time consumption of the DC sweep simulations (for V_{CE} going form 0 to 20V with a step of 0.1V and fixed V_{BE}) with the Synopsys's HSPICE for two transistors with the different inner matrix dimensions is shown in Table 1.

	Reduced Model	Full Model
20×20 matrix	0.60 sec.	1.05 sec.
32×32 matrix	2.54 sec.	5.67 sec.

Table 1: Computation (CPU) time

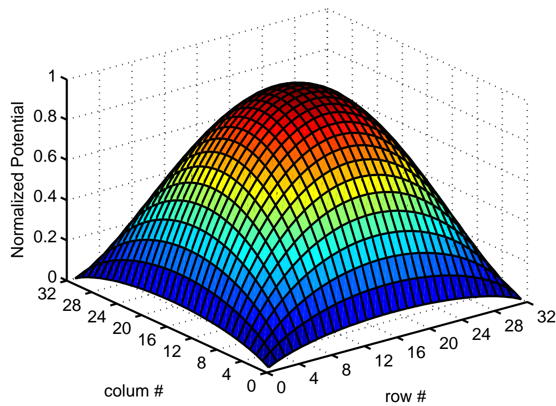

Figure 7: Intrinsic base potential (relative to emitter metal contact) distribution obtained by segmentated transistor model simulation in avalanche regime.

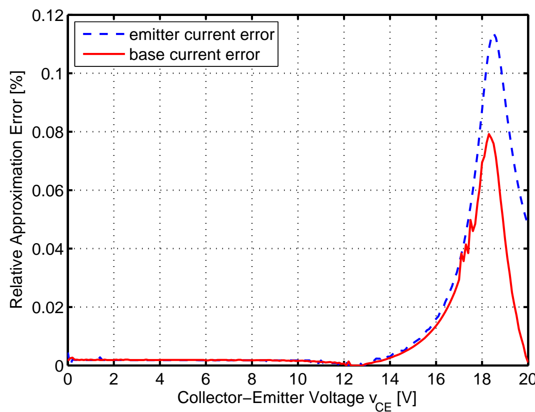

Figure 8: Relative approximation error for the base port and the emitter port current in a DC sweep simulation.

Computation time is at that particular case halved in comparison to the original segmentated model. The achievable computational gain depends on the size of the transistor matrix and in ideal situation should be a linear function of the matrix dimension. In practice, the computational complexity is expected to rise faster than linear but also slower than quadratic function of the input matrix dimensions.

4 CONCLUSION

A reduction technique for an accurate modeling of complex effects manifested in the avalanche regime of a bipolar junction transistor is presented in this paper. Phenomenon that is well known but still not included in any of the today's compact models is discussed first. Already existing quasi-distributed 3-dimensional transistor model is evaluated and its weakest point, the complexity, is emphasized. A simplification method that utilizes a normalized bilinear approximation is described. A rudiments of this method are explained in details and the model is practically implemented in Verilog-AMS language. The model implementation is based upon Mextram. The additional parameter necessary for the full model definition is pointed and its extraction technique is portrayed. The quantitative and comparison (with currently available model) results are discussed. The results are showing the significant gain in calculation time without notable loss in the accuracy. Excellent agreement between the simulated and the experimental results is achieved.

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