

Methodology & Design Kit Integration of a Broadband Compact Inductor Model

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ABSTRACT

On-chip inductors are widely used in many modern RFICs. Realization of high-Q inductors often requires extra back-end processing and costly chip area. Accurate modeling and thorough optimization of the inductor are required for best performance. In this paper we present a scalable broadband inductor model. The model supports multiple symmetric and asymmetric inductor layouts and has been incorporated into IBM Process Design Kits for a wide range of technologies.

Keywords: inductor, compact model, RF, skin effect, proximity effect.

1 INTRODUCTION

The model is a translation from the inductor geometry definition to a network (Fig. 1) that captures the electromagnetic behavior of the device. The inductor geometry is defined by a set of geometric parameters such as trace width (w) and spacing (s), number of turns (n), outer diameter (x), and stacking option ($stack$). The stacking options indicating what type of inductors are being modeled is shown in Fig. 2 (ind, indp, inds, symind, symindp). In addition, one or more parameters (tlev1, tlev2, tlev3,...), dependent on technology definition, are used to indicate the number and thickness of each different metal level that exists in the Back End of Line (BEOL) metallization. The passed in tlev values define a specific arrangement of conductors for the spiral: number and type of metal levels connected in parallel and number and type of metal levels comprising the underpasses. A statistical modeling methodology is implemented utilizing a separate file (skew file) containing process parameters that are common to multiple different device types (i.e. metal sheet ρ , dielectric thickness, temperature coefficient of resistance, line width bias,...). Each of these parameters in the skew file is assigned a statistical distribution and the resulting values are used in all models, ensuring that the devices remain correlated during statistical analyses. The final geometry of each metal shape and dielectric level comprising the spiral is either the nominal or the statistically perturbed value depending on the type of simulation being requested.

Scalability & Optimization: For a typical inductor application, there is often a target inductance value, along with a minimum tolerable quality factor, and maximum

area available / affordable for the inductor. The target inductance can be achieved by multiple combinations of inductor geometry parameters, however, only a handful of the combinations are optimal in the sense that they produce high Q or minimize area. A scalable model allows the exploration of the design space through iterative simulations from which the optimum geometry meeting the target specifications can be extracted.

Broadband Accuracy: Current flow is not uniform across the width and the thickness of the inductor metal due to skin and proximity effects. This leads to frequency dependent resistance and inductance to be captured by the inductor model. While other inductor models have used network elements with frequency dependent values ($R(f)$ and $L(f)$), such an approach requires knowledge of the frequency of operation [1,2]. This method cannot be used for transient (TRAN) and periodic steady state (PSS) analyses required for the simulation of RF circuits such as VCOs and others. A preferred solution is the utilization of an R-L ladder network with effective frequency dependent resistance and inductance, valid for all types of analyses. In addition to metal loss, as the frequency of operation increases, the inductor Q is limited by the losses in the semiconductor substrate. The shunting effect of the trace-to-trace and trace-to-substrate capacitances determines the self-resonance frequency of the inductor. The model must capture the aforementioned effects correctly for simulation accuracy at radio frequencies.

2 BROADBAND RESISTANCE & INDUCTANCE MODELING

Accurate modeling of the frequency-dependent loss mechanisms present in the metal turns of the spiral inductor is essential in correctly reproducing the spiral's broadband behavior. Both low and high frequency loss effects must be accurately modeled as well as statistical variations and temperature effects. Once the final geometries are known, taking into account statistical variation if desired, the DC resistance and inductance of the spiral can be calculated. The model is represented with a distributed two- π topology. In the case of a symmetric spiral, the model treats each half of the spiral separately before combining them into the final two- π representation. Each π section contains a skin effect network and a proximity effect network. The two halves of the spiral are then coupled together with seven coupling coefficients relating the two skin effect networks and the two outer inductances (see Fig. 1).

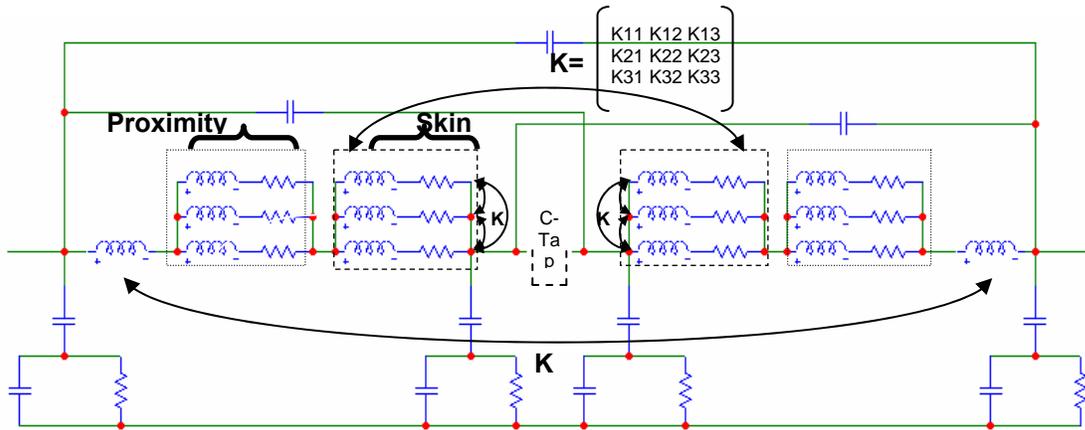


Fig. 1. Passive network used by the model.

Many techniques have been suggested to model the skin effect influenced frequency dependent behavior of a conductor [1,2,4,5]. The IBM model uses a purely physical approach. The skin effect network is calculated by treating the $\frac{1}{2}$ spiral as one long, straight conductor in free space with the same dimensions as the spiral turn (length, conductivity, width and thickness). The conductor is partitioned into nested rectangular annuli and the inductances (self and mutual) and resistances of each annulus are calculated. The resulting R-L ladder network with mutual coupling will replicate the broadband skin effect behavior with increasing accuracy as the number of partitions is increased. We have determined that three partitions are sufficient to represent the frequency-dependent behavior from DC to 40GHz with very little error. Calculating the self and mutual inductances of an annulus with a rectangular cross-section is difficult without resorting to numerical techniques. In order to facilitate the calculation of the inductances within the compact model, a different approach is required. It was recognized that nested, circular annuli had closed form solutions for inductance and mutual coupling [3]. In order to use these closed form solutions, the rectangular cross-section needs to be transformed into a circular cross-section (see Fig. 3). This is achieved by equating the closed form equation for the self inductances of circular and rectangular cross-section conductors and calculating the required equivalent radius [3]:

$$R_{equiv} = \frac{0.2235 \cdot (w + t)}{0.7788} \quad (1)$$

Once the equivalent cylindrical geometry is known, all that remains is to choose a partitioning scheme that can effectively capture the current density expected to flow in the cylindrical conductor. Narrow partitions at the outer

surface with progressively larger partitions toward the center of the conductor help to capture the skin effect accurately. This can be done by equating the outermost partition dimension to the skin depth at the highest frequency of interest through a proportionality constant (α) [4]:

$$\alpha = \frac{0.53 \cdot R_{equiv}}{\delta_{max}}, \text{ with } \delta_{max} = \text{skin depth at 40 GHz} \quad (2)$$

In order to calculate the geometries of the remaining annular partitions, a constant ratio relating the resistance of the outer annulus to the next annulus in and finally to the central cylindrical conductor (3 partitions) is assumed (see Fig. 3). These three equations are solved for the resistance ratio (RR) using the quadratic formula:

$$RR = \frac{\sqrt{1 - 4 \cdot (1 - \alpha)} - 1}{2} \quad (3)$$

Once this is known, the physical geometry of each annular subsection can be calculated from knowledge of its resistance and conductivity. From the physical geometries of each annular section, the self and mutual inductances can be calculated in closed form. This yields the complete broadband skin effect model used in the inductor model of Fig. 1 and detailed in Fig. 3.

The proximity effect network consists of an R-L ladder network (similar to the skin effect network but without the mutual inductances). This network is designed to empirically mimic the proximity effect behavior (negligible additional inductance and resistance at low frequency with an inductance drop and resistance increase with increasing

frequency). This network's behavior is fitted to the measured characteristics of a large variety of inductor geometries utilizing fitting coefficients that primarily depend on the "hollowness" of the spiral of interest. Very hollow spirals experience small proximity effect and very filled-in spirals experience dramatic proximity effect. The combination of skin and proximity effect networks provides the needed frequency dependent loss behavior to accurately predict the broadband Q and inductance behavior of a wide range of spiral geometries.

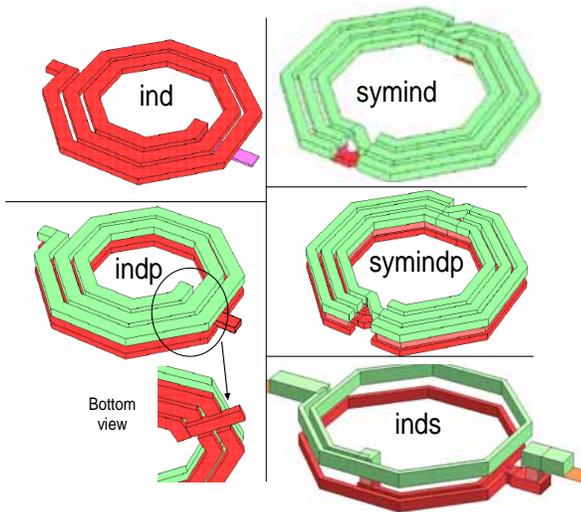


Fig. 2. Layout configurations supported by the model.

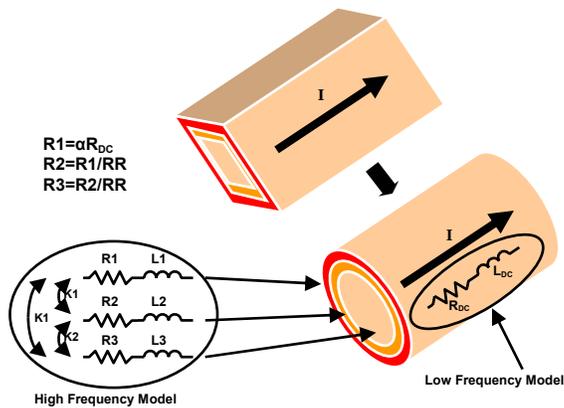


Fig. 3. Cross-section partition based on skin depth, resistance ratio (RR), and # of desired subsections.

3 CAPACITANCE NETWORK & SUBSTRATE MODELING

On-chip inductors are only separated from the semiconductor substrate by about 1-15 μ m of dielectric films. The traces are often laid out at the minimum spacing allowed by the ground rules, with the goal of maximizing

inductance density. The capacitive interaction within the inductor traces and between the inductor and the substrate is modeled through a partially distributed capacitance network.

A 2D quasi-static capacitance calculator is employed to extract the capacitance matrix for a system of six metal lines as a function of height and metal separation (Fig. 4). Area and fringe capacitance equations are fitted to the resulting capacitance matrices. Separate equation sets are extracted for isolated traces, embedded traces, and overlapping traces. The capacitance calculations are run for the various metallization combinations to be captured by the inductor model. In a modern Copper process, each metal may be surrounded by films of various thicknesses and permittivities. The different dielectric properties of the materials are accounted for in the calculations. Area and length of the inductor traces are computed in the model, and the total capacitance is calculated using the extracted functions. Impact of dummy metal fill is included in the model by means of an effective height calculation which assumes that fill shapes will influence the electric field within twice the fill area. The computed capacitance is then distributed within the network (Table I).

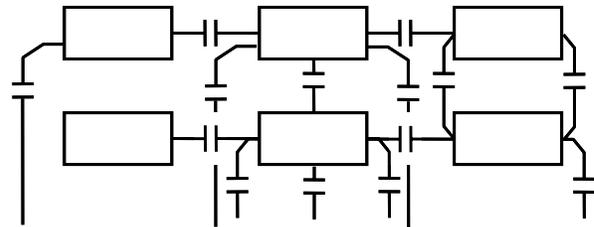


Fig. 4. Extracted capacitance matrix used by the model.

Table I: Description of model elements.

Network elements:	To model:
2 R-L-K networks	the variation in inductance and resistance due to skin and proximity effects
9 mutual inductances	the magnetic coupling between primary and secondary halves of the spiral
2 coupled series inductors	the extra inductance due to magnetic coupling between the two halves
2 series resistors	the underpass
3 capacitors	the metal-to-metal capacitive coupling among the inductor traces
4 capacitors	metal-to-substrate capacitive coupling
4 capacitors & 4 resistors	the dielectric and loss behavior of the semiconductor substrate

The substrate loss is modeled with a resistor network in series with the inductor-to-substrate capacitance. The presented model also supports a Faraday shield groundplane option, where a low resistance groundplane is placed underneath the inductor [5]. The groundplane captures most of the electric field emerging from the inductor before it enters the substrate. This minimizes losses in the substrate increasing peak Q value. However, the inductor self-resonance frequency is reduced due to increased capacitance. These effects are captured in the model by modifying the RC network representing the dielectric and the substrate.

4 SUMMARY

In summary, a physics based broadband scalable inductor model is presented. It can be used in an iterative optimization flow to determine the best geometry for target inductance and quality factor. The model supports various symmetric and asymmetric layout topologies suitable for different applications. The model has been integrated into process design kits and has shown remarkable hardware correlation (e.g. Fig. 5.) for a wide range of technologies with various substrate types, dielectric heights, and metallization options.

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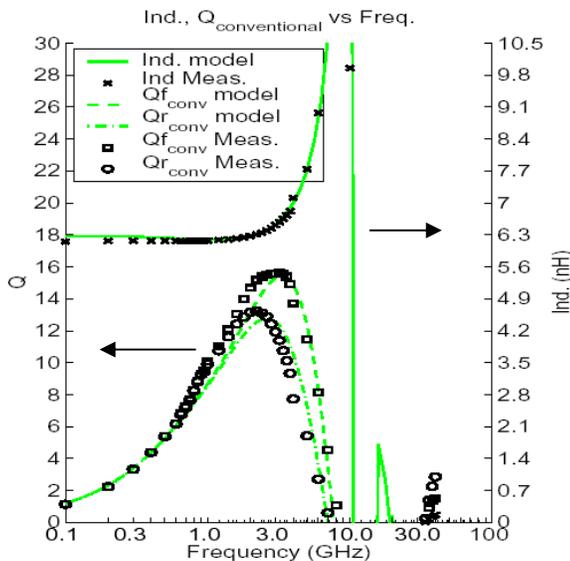


Fig. 5. Example hardware correlation of the model.