HiSIM-Varactor: Complete Surface-Potential-Based Model for RF Applications

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Abstract

For RF-circuit analysis, an accurate compact model for the MOS varactor is urgently desired. We have developed such an accurate MOS varactor model HiSIM-Varactor based on the surface-potential MOSFET model HiSIM by considering the majority carrier transit time. Good agreement with 2D device simulation result is verified up to 200GHz operation. The calculated quality factor is proved to deviate from linearity as a function of operation frequency due to the capacitance-formation delay caused by the carrier transit delay.

Keywords: MOS-varactor model, RF applications, surface-potential-based model, NQS effect, quality factor

1 Introduction

Voltage-controlled oscillators (VCOs) are keys in RF circuits [1]. For the frequency tuning of the VCOs, integrated varactors are applied to provide voltage-dependent capacitances. It has been demonstrated that MOS-type varactors offer a frequency tuning range by changing the operation range of MOS transistors [3]. A high Q (quality factor) is also achievable. Many investigations have been carried out to achieve a wide tuning range with conventional MOSFET technologies [4]–[6], in which different operation modes, either the inversion mode or the accumulation mode, have been developed [7]. Inversion-mode MOS varactors are constructed in a similar manner to normal MOSFETs, whereas accumulation-mode MOS varactors consist of the same impurity type for source/drain contacts and wells, as shown in Fig. 1a, leading to the lack of sources for supplying inversion layer carriers. Therefore, the inversion condition can never occur in the RF operation of the accumulation-mode MOS varactors.

Although the importance of the MOS varactors is very high, accurate models for RF applications are still missing. To apply the MOS varactors to an RF regime, not only the voltage dependence but also frequency dependence of the MOS capacitance has to be accurately predicted. In a high-frequency operation, a non-quasi-static effect suppresses the capacitance [8]. Additionally, little attention is paid to modeling the accumulation region for the circuit application of normal MOSFETs. Thus, our aim is to develop an accurate MOS-varactor model operating in the accumulation mode applicable for RF circuit simulations. The model is developed as an extension of HiSIM (the Hiroshima-University STARC IGFET Model) [9], [10] and named the HiSIM-Varactor.

2 Feature of Studied MOS Varactor

The feature of the MOS varactor is that it induces no inversion condition. The contacts corresponding to the source, drain and bulk in a conventional MOSFET (see Fig. 1b) are connected together and a bias is applied between the gate contact and the connected contact, $V_{\rm gb}$ (see Fig. 1a). The third contact to the substrate is also used to achieve a high varactor performance. By applying a bias to the substrate, the accumulation region has been shown to provide a more stable and wider tuning range than without [11]. Here, we study a two-port application, and thus, the resistance effect induced at the n/p junction is not considered.

Since the MOS-varactor function is based on the tunable capacitance induced by applying the voltage $V_{\rm gb}$, an accurate capacitance modeling is inevitable for predicting the MOS-varactor performance accurately. Figure 2 shows the MOS-varactor 2D-device simulation results at different frequencies. The rapid decrease in capacitance around $V_{\rm gb} = -1.5$V for very low frequencies is due to the deformation of an inversion layer, whereas the gradual increase beyond $V_{\rm gb} \simeq -0.5$V represents the formation of the accumulation condition. Under the DC condition, the inversion layer is formed thermally, and the MOS varactor has the same capacitance characteristic as a normal MOSFET. A negligible increase in operation frequency changes the characteristic, and the inversion condition never occurs, maintaining the capacitance at its minimum. However, the characteristic beyond the depletion region ($V_{\rm gb} > -1.5$V) is not changed for low frequencies.

3 Modeling Approach

For our study, MOS-varactor dimensions are fixed to be the width W and length L of W/L=1 μm/2 μm, and

impurity concentrations are fixed to be typical literature values, as given in Fig. 1a.

3.1 At low frequency

The feature of the MOS varactor shown in Figure 2 is modeled with the Poisson equation with the minority carrier density $p_{\rm n}$ of which decreases to zero in an AC operation.

$$\frac{\partial^2\phi}{\partial x^2} = -\frac{q(N_{\rm D} - n_{\rm n} + p_{\rm n}(\rightarrow 0))}{\epsilon} \tag{1}$$

Here, ϕ is the potential, and $N_{\rm D}$, $n_{\rm n}$, and $p_{\rm n}$ are the acceptor, electron, and hole densities, respectively. The permittivity of the Si substrate is denoted by ϵ, and the x denotes the direction vertical to the surface. Thus, the basis of the HiSIM-Varactor is the surface potential ϕ, the same as that of the HiSIM for bulk MOSFETs. The charges induced by the applied voltage $V_{\rm gb}$ are described as a function of the surface potential calculated by solving the Poisson equation given in Eq. (1). The depletion and accumulation charges are the charges induced by $V_{\rm gb}$, which are the origins of the gate capacitance $C_{\rm gg}$. A calculation result with HiSIM-Varactor is shown in Fig. 3, together with a 2D-device simulation result. A good agreement is observed.

3.2 At high frequency

Figure 4 shows the 2D-device simulation results for $C_{\rm gg}$ by symbols in different frequency operations. Beyond 10 GHz, the calculated capacitance starts to decrease with an increase in frequency. This is more obvious in the accumulation region. This reduction is attributed to the non-quasi-static (NQS) effect [14]. Majority carriers take time to form the accumulation layer. The NQS model of the HiSIM for the MOSFET considers that the delay τ consists of the carrier transit delay for the inversion charge and the charging delay for the bulk charge. The delayed charge formation is modeled with the delay as [15]

$$q(t_{\rm i}) = q(t_{\rm i-1}) + \frac{\Delta t}{\tau + \Delta t}\Big(Q(t_{\rm i}) - q(t_{\rm i-1})\Big);\ \Delta t = t_{\rm i} - t_{\rm i-1}, \tag{2}$$

where $q(t_{\rm i})$ and $Q(t_{\rm i})$ represent the NQS and QS charge densities at the time $t_{\rm i}$, respectively. The capacitance $C_{\rm gg}$ calculated with the HiSIM for a bulk MOSFET is shown in Fig. 5 in different frequency operations. The capacitance reduction in the inversion region, as well as that in the accumulation region, is markedly enhanced. For the MOS varactor, the majority carriers move mainly from the two $n+$ contact regions. Thus, the NQS model of the HiSIM-Varactor considers the majority carrier charging delay τ. Discharging under the depletion condition is also modeled separately. The former is called the accumulation delay $\tau_{\rm acc}$ and the latter $\tau_{\rm dep}$, which are basically the functions of the channel length, where carriers flow, and the carrier velocity.

$$\tau = \frac{L/2}{v} \tag{3}$$

Here v is the carrier velocity. The carrier velocity v is dependent on the applied field.
The field consists of two components, E_x (vertical to the surface) and E_y (parallel to the surface). E_x is determined by the applied voltage $V_{\rm gb}$, whereas E_y by the built-in potential at the contact/n-well junction. However, E_x dominates E_y, thus

$$E = \sqrt{E_x^2 + E_y^2} \simeq E_x \tag{4}$$

Figure 6 shows the simulated surface E_x in the middle of the channel as a function of $V_{\rm gb}$. Under the flat-band condition ($V_{\rm gb} = V_{\rm fb} = -0.12$ V), the field decreases to zero and its sign changes, corresponding to the switching from the depletion condition to the accumulation condition. The sign of E_x controls the gathering of majority carriers on the surface (charging) or their departure from the surface (discharging). The channel-length-independent delays $\tau_{\rm A}$ and $\tau_{\rm D}$ are modeled by exponential functions with the model parameters *A*-*F* after the field feature shown in Fig. 6.

$$\tau_{\rm D} = A \cdot \exp\big(B \cdot (V_{\rm gb} - V_{\rm fb})\big) + C \tag{5}$$
$$\tau_{\rm A} = D \cdot \exp\big(E \cdot (V_{\rm fb} - V_{\rm gb})\big) + F \tag{6}$$

Here,

$$\begin{aligned} \tau_{\rm dep} &= L \cdot \tau_{\rm D} \\ \tau_{\rm acc} &= L \cdot \tau_{\rm A} \end{aligned} \tag{7}$$

The two delay mechanisms described by $\tau_{\rm dep}$ and $\tau_{\rm acc}$ are then combined by the Matthiessen's rule for the effective delay τ.

$$\frac{1}{\tau} = \frac{1}{\tau_{\rm dep}} + \frac{1}{\tau_{\rm acc}} \tag{8}$$

4 Calculation Results and Discussion

Figure 4 shows a comparison of calculation results (lines) with the developed model and the 2D-device simulation results (symbols). Good agreement in all frequency operations is achieved. The reduction in capacitance in a high-frequency MOS varactor operation shows the loss of the tuning capability of the VCO during oscillation. This limits the MOS-varactor functionality.
The quality factor Q is an important measure for verifying the performance of the MOS varactor and is defined as

$$Q = \frac{1}{2\pi f \cdot R_{\rm p} \cdot C_{\rm gg}}, \tag{9}$$

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where $R_{\rm p}$ is the parasitic resistance [3]. Sometimes, the inductance is included in the definition for high-frequency analysis. However, in this study, we concentrate on the NQS effect on the quality factor, such that a simple definition is applicable. Figure 7 shows Q multiplied by $R_{\rm p}$ as a function of frequency at $V_{\rm gb} = 1$V. In a double-log plot, $Q \cdot R_{\rm p}$ is proportional to frequencies up to 10 GHz. At frequencies higher than 10 GHz, Q starts to deviate from the linear dependence. This is caused by the $C_{\rm gg}$ reduction due to the NQS effect.

5 Conclusions

For RF-circuit analysis, an accurate compact model for MOS varactors is urgently desired. We have developed a MOS-varactor model HiSIM-Varactor on the basis of the surface potential description of the HiSIM for MOSFETs, enabling the seamless calculation of capacitance from the depletion condition to the accumulation condition. Good agreements are verified for operation frequencies up to 200 GHz with 2D device simulation results. It is shown that the MOS-varactor model has to include the non-quasi-static effect explicitly for predicting the features of the MOS varactor in RF operations.

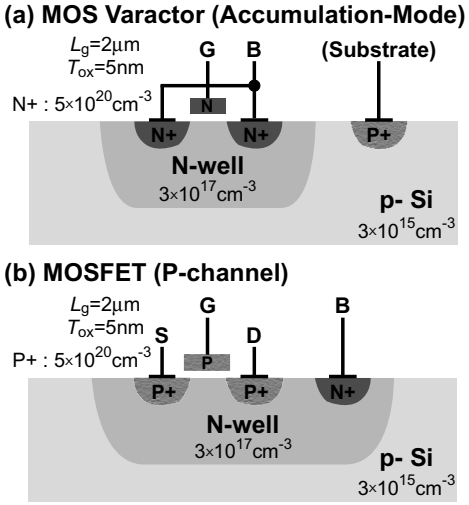

Fig. 1: Schematic device structures: (a) studied MOS varactor and (b) conventional p-MOSFET for comparison.

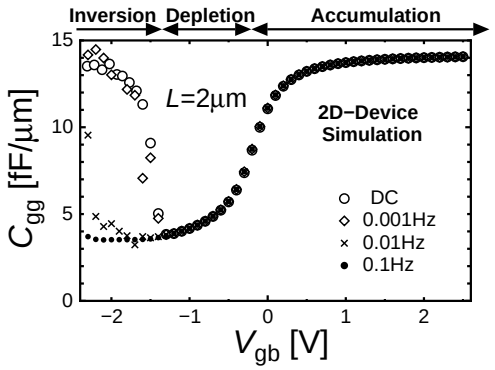

Fig. 2: Simulated $C_{\rm gg}$ values of MOS varactor in different frequency operations.

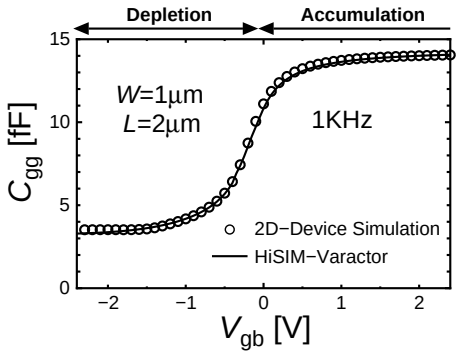

Fig. 3: Calculated gate capacitance $C_{\rm gg}$ of MOS varactor as function of applied voltage $V_{\rm gb}$. For comparison, the results obtained by 2D-device simulation are also shown.

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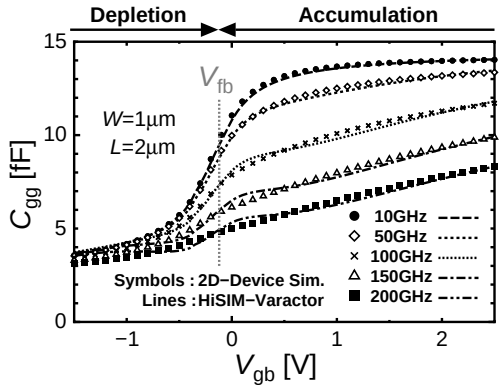

Fig. 4: Comparison of calculated C_{gg} values of HiSIM-Varactor and 2D-device simulation results at different operation frequencies.

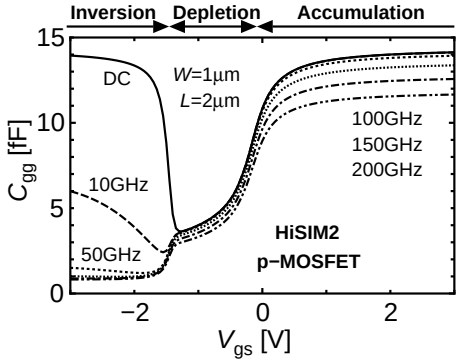

Fig. 5: Calculated gate capacitances of p-channel MOSFET with HiSIM2-NQS model at different frequencies.

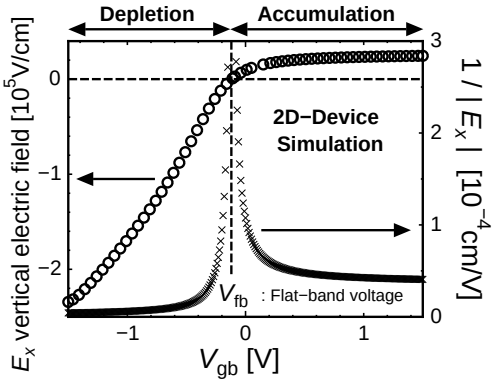

Fig. 6: Simulated electric field vertical to surface E_x and its inverse obtained by 2D-device simulation as functions of applied voltage V_{gb}. These values are obtained in the channel middle slightly below the surface.

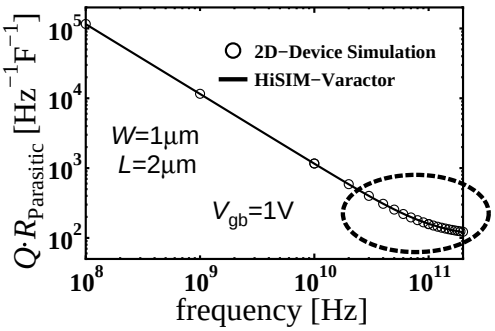

Fig. 7: Calculated quality factor as a function of operation frequency for the developed model, HiSIM-Varactor. The results of multiplying the quality factor with the parasitic resistance are depicted. 2D-device simulation results are also depicted for comparison. The dashed oval shows the NQS effect, causing a deviation from the linear dependence.

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