HiSIM2.4.0: Advanced MOSFET Model for the 45nm Technology Node and Beyond

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Abstract

HiSIM realizes both accurate and fast circuit simulation. The HiSIM2 version includes required features in modeling for the 45nm technology node and beyond such as the STI effect. A major development is an improved model consistency, which enables even modeling of the technology variation accurately. HiSIM2.4.0 includes also the binning option to take into account newly appearing device features which are not modeled yet.

Keywords: MOSFET model, surface potential, analog & RF application, calculation speed

1 Introduction

The compact MOSFET-model development trend leads to models based on the channel surface potential, allowing higher accuracy and a reduced number of model parameters in comparison to the threshold-voltage-based models [1]–[3]. This is reflected in the fact that most of multi-gate MOSFET models, being intensively developed nowadays, are based on the surface potentials [4]–[6]. It has been demonstrated that excellent model accuracy for higher-order phenomena as well as noise features, which is a prerequisite for accurate RF circuit simulation, has been achieved by the surface-potential-based modeling without any new model parameters in addition to those for describing the I-V characteristics [1], [7]. The main reason for such successful achievement is the consistency in describing measured phenomena. Only one measure, namely the surface-potential distribution along the channel, is treated to be the origin of all device features. This is also the basis of the real device physics [8], [9].

There are different approaches within the surface-potential-based modeling in how to calculate the surface potentials from the Poisson equation: One is to solve iteratively [1] and the other is to calculate with simplified analytical equations [2], [3]. Among existing models available for actual applications only HiSIM (Hiroshima-university STARC IGFET Model) solves the surface potentials with the iteration procedure, avoiding additional approximations without any computer run-time penalty [11], [12].

MOSFET technology is leading semiconductor industries through aggressive size reduction on a short time scale. In addition to the performance improvement of MOSFETs by scaling, many descendants such as LDMOS have been developed to realize required circuit performances and applications [10]. Another aspect to be considered in modeling is thus extendability to all possible structures. A big advantage of the modeling approach based on the principle of device physics is that it allows to apply the model to all kinds of MOSFET structures with a single set of basic equations. Capabilities of HiSIM2.4.0 will be overviewed here.

2 Accuracy of Calculation Results

The main objectives of our efforts are to obtain:

- a limitation to the parameter inflation by providing only one parameter set for all channel lengths of the MOSFET
- highly accurate reproduction of the $I-V$ characteristics of the MOSFET including all secondary effects of advanced technologies, which are becoming dominating, and source-drain symmetry
- high accuracy of the derivatives of the $I-V$ characteristics up to 3rd order
- RF simulation capability by accurate intrinsic capacitance, noise and non-quasi-static (NQS) models
- a binning option for considering not yet modeled effects and keeping the model flexible
- short simulation times as good or better than the conventional $V_{\rm th}$-based models

The surface potential is calculated with the Poisson equation [8], [9], which is an implicit function of the surface potential. Therefore, HiSIM solves the equation iteratively in the same way as numerical device simulators but with a quasi 2D algorithm. To achieve fast calculation speed, good initial guesses for the iteration as well as an appropriate algorithm for the Newton iteration

are keys. As a result the simulation time with the iterative approach turns out to be faster than with the non-iterative approach [11], [12], because the iteration number can be kept small and because the calculated quantities in the iteration loop remain simpler. Calculated surface potentials and their derivatives are shown in Fig. 1.

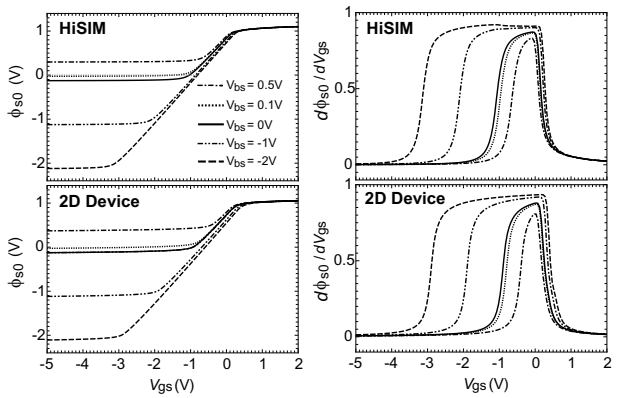

Fig. 1: Comparison of calculated surface potentials at source side ϕ_{S0} and their derivatives by HiSIM2 and a 2D-device simulator for various substrate voltages $V_{\rm bs}$ at a drain voltage of $V_{\rm ds}$=0.1V. Gate length is fixed to 2μm.

Fig. 2 shows calculated $I-V$ characteristics with HiSIM2 in comparison with measurements for a 65nm technology. The shortest gate length $L_{\rm g}$ of 40nm. A single model-parameter set is valid for all gate length. Fig. 3 compares higher-order derivatives of the transconductance $g_{\rm m}$ for two drain voltage ($V_{\rm ds}$) values. Good reproduction of all higher-order derivatives for any bias condition is due to the unified modeling approach based only on the surface potentials.
Fig. 4 shows Gummel symmetry tests up to 3rd derivatives. The source-drain symmetry of MOSFETs is important in circuits, where the operating point of MOSFETs swings through $V_{\rm ds}$ = 0 [13], [14]. The surface-potential-based modeling preserves the source-drain symmetry at $V_{\rm ds}$=0 in principle automatically. However, the fundamental nature of this symmetry can be affected by the modeling of advanced MOSFET phenomena such as short-channel effects. In HiSIM2 efficient numerical damping is used to suppress such negative effects from advanced MOSFET-phenomena modeling.

3 STI Effect

The shallow-trench-isolation (STI) technology is commonly used in advanced device fabrication. However, it induces a stress to the device substrate [15], which causes modification of the MOSFET characteristics from the original ones. This is modeled by considering the

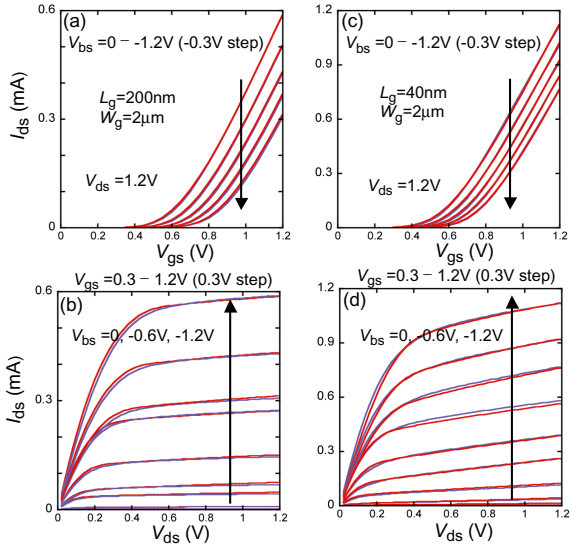

Fig. 2: Comparison of calculated $I-V$ characteristics with HiSIM2 (red lines) and measurements (blue lines) for $L_{\rm gate}$=200nm (a) $I_{\rm ds}$ vs. $V_{\rm gs}$ (b) $I_{\rm ds}$ vs. $V_{\rm ds}$ and for $L_{\rm gate}$=40nm (c)$I_{\rm ds}$ vs. $V_{\rm gs}$ (d) $I_{\rm ds}$ vs. $V_{\rm ds}$.

distance from the gate edge to the STI edge [16]. However, accurate modeling of the leakage current causing additional current flow at corners of the device is a prerequisite. This leakage current even dominates over the original current for very narrow devices as shown in Fig. 5. In future modeling of such kind of currents is expected to become the main task.

4 Simulation Speed Issues

An important objective for the development of compact models is a short computer runtime of the model, because circuit designers need to carry out even analog simulations of circuits with large transistor numbers nowadays. Even for DRAM circuits, using very aggressive technologies, require high accuracy of device models to fulfill aggressive design tasks. The transistor-number requirements for circuit simulation have been increasing with technology generations, due to the possibility of placing more and more transistors on a single chip, and have recently crossed the barrier of 1 million transistors. The simulation-speed objective was one major reason for the choice of the conventional threshold-voltage-based modeling approach, implemented in the Meyer model and also in the widely used BSIM model series, because it was assumed that approaches with fewer approximations and therefore higher accuracy, like the surface-potential approach, would inevitably lead to an intolerably large computer-runtime penalty. However, with advancing scaled-down fabrication technologies the necessity of including explicitly induced phenomena like short-channel effects, noise effects, NQS effects or non-

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

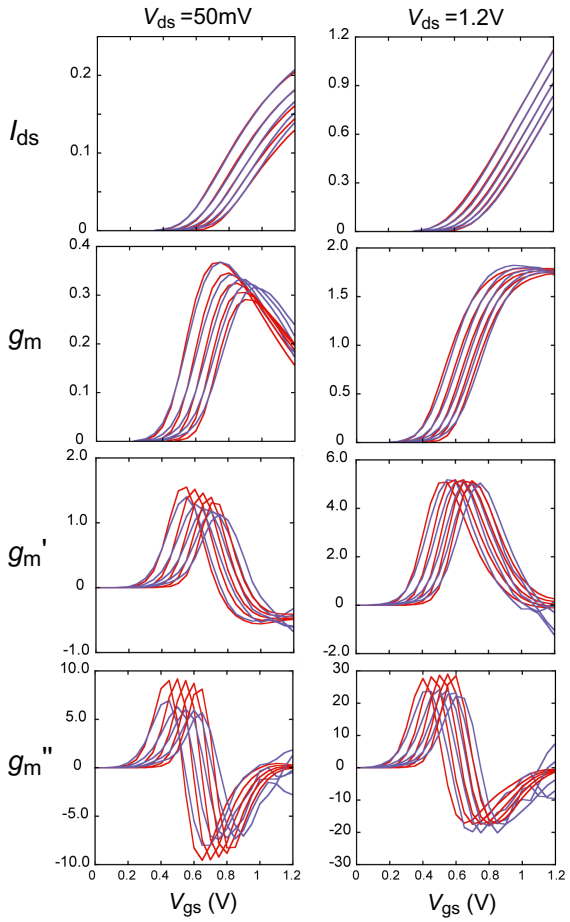

Fig. 3: Comparison of HiSIM2 results (red lines) and measurements (blue lines) for I_{ds} derivatives at small and large V_{ds}. The MOSFET dimensions are L_g=40nm and $W_g = 2\mu m$.

homogeneous channel doping into the compact models, became a high burden for the threshold-voltage-based models, leading to large number of fitting parameters and a strongly increasing computer runtime. On the other hand, non-negligible induced effects in advanced technologies could be included into the more physical surface-potential-based models like HiSIM in a much more natural and less calculation-time-expensive way [17]. Consequently, already HiSIM231 featured even shorter circuit-simulation times than BSIM4.

HiSIM requires two iteration steps for calculating two surface potentials. One is the surface potential at the source side ϕ_{S0} and the other is the surface potential at the drain side ϕ_{SL}. The calculation speed of HiSIM is verified by measuring the simulation time for each calculation step. Fig. 6 shows the CPU time variation as a function of the gate voltage V_{gs} for a fixed drain voltage of V_{ds}=0.1V. The CPU time was measured by repeating the DC simulation for 200 times at each bias condition, and the simulation times at four different steps in the

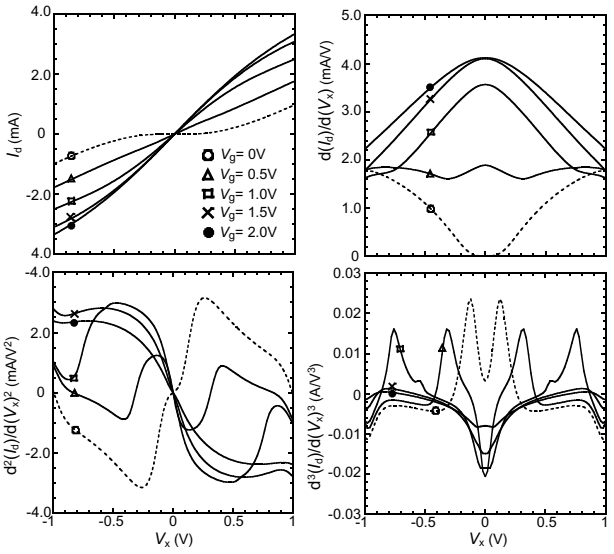

Fig. 4: Gummel symmetry test for I_{ds} up to the 3rd derivative.

HiSIM code were measured. The result is shown cumulatively. The fluctuation of the measured CPU time is due to the computational condition fluctuation during the measurement. The line 4 shows the total simulation time including all leakage contributions, and the line 3 is the end of the simulation time for the intrinsic part. The line 1 and 2 are the end of the iteration steps for ϕ_{S0} and ϕ_{SL}, respectively. the sum of the internal iteration steps is less than 20% of the total simulation time. In the threshold voltage based model there is no burden of such an iterative simulation time. However, the simulation time for the intrinsic part, the difference between the line 2 and the line 3, is kept low in HiSIM due to simple description of the device characteristics. As a result total simulation time compensates the burden of the simulation time caused by the iteration procedures. Thus an important feature of the surface-potential-based model is that it requires not much simulation time, once the surface potentials are calculated.

As can be seen in Fig. 6, the total simulation time is not dominated by the surface-potential calculation but other calculation steps take the main share of the overall calculation time. Table 1 shows a comparison of iteration numbers required in circuit simulation with SPICE3f5 for various simple test circuits [18] with HiSIM240 and BSIM450. The comparison is done with default model parameter values for both models. The number of iteration steps denotes the smoothness of model equations. If the model equations are smooth and no abrupt changes exist in device characteristics as a function of applied biases, the number of iterations is kept small. To accomplish complete smoothness for any bias conditions, even for the conditions where no device physics is valid any

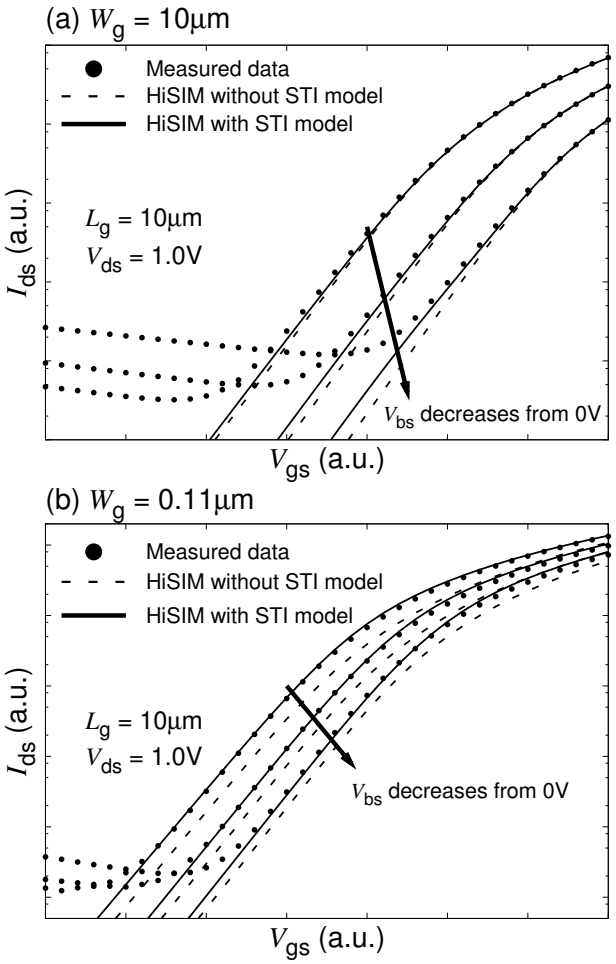

Fig. 5: Comparison of the I-V characteristics for the gate width W_g of (a) 10μm and (b) 0.11μm. The gate length L_g=10μm.

more, compact models normally apply many smoothing functions. This can be minimized by modeling with the surface potentials.

Table 1: Comparison of Iteration Numbers in Circuit Simulations with HiSIM and BSIM.

Circuit	HiSIM240	BSIM450
cram	2204	2286
mux8	21176	23011
ring	4778	6056

5 Modeled Phenomena

Table 1 summarizes all phenomena modeled in HiSIM2. Most of the phenomena are observed in any type of device geometries for advanced technologies.

Figs. 7-9 show simulation results with HiSIM for the flicker noise, the thermal noise, and the induced-gate noise, respectively [19]–[21]. It has to be noted that no additional model parameter is required for the simulations, but measured I-V characteristics simulate automatically the results, if the technology is already mature.

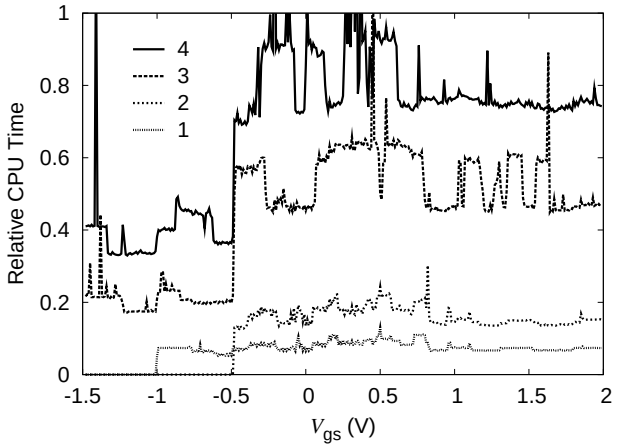

Fig. 6: CPU times needed for HiSIM2.4.0 to calculate: Ps0 calculation (short-dashed line), Psl calculation (dotted line), basic characteristics (dashed line), and complete program (solid line). One PC with Fedora Core Linux 6 and Intel Pentium 4 CPU 3.40GHz is used.

Table 2: Modeled phenomena in HiSIM.

Phenomena	Subjects
Short Channel Reverse-Short Channel	 impurity pile-up pocket implant
Poly-Depletion Quantum-Mechanical Channel-Length Modulation Narrow-Channel	
Non-Quasi-Static	Transient Time-Domain AC Frequency-Domain
Temperature Dependency	Thermal Voltage Bandgap Intrinsic-Carrier Concentration Phonon Scattering Maximum Velocity
Mobility Models	Universal Mobility High-Field Mobility
Shallow-Trench Isolation	Threshold Voltage Mobility Leakage Current
Capacitances	Intrinsic Overlap Lateral-Field Induced Fringing
Noise	1/f Noise Thermal Noise Induced Gate Noise Cross-Correlation Noise
Leakage Currents	Substrate Current Gate Current GIDL Current
Source/Drain Resistances Junction Diode	 Currents Capacitances

HiSIM240 provides binning options, where possible model parameters for the binning are limited for model parameters directly connected to device parameters in the first option. However, a second option for extending the binning possibility is also provided to keep flexibility.

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

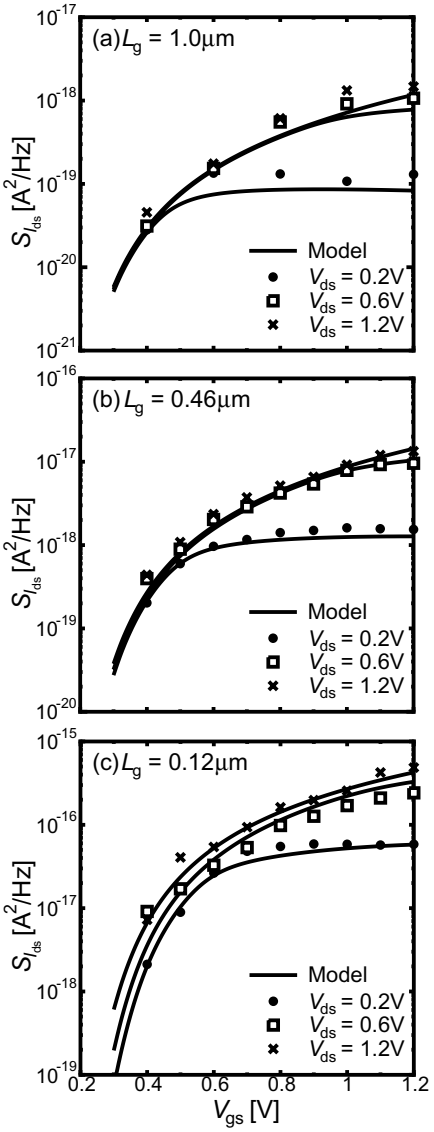

Fig. 7: Calculated $1/f$ noise characteristics in comparison with measurements. Only the trap density $NFTRP$ is the model parameter, valid for all gate lengths. If the technology is manure the value is universal.

6 CONCLUSION

The development trend in compact modeling goes towards surface-potential-based approaches and leads to models like HiSIM2, with higher accuracy, fewer model parameters and shorter computer runtime than achievable with the conventional threshold-voltage based approaches. The main motivation for continuing this development effort is to realize a sufficient design capability of RF-circuits with advanced MOSFETs, where many higher-order phenomena affect the circuit performance, as well as of large mixed-signal circuits, where both accuracy and short simulation time are a must. The trend toward the surface potential brings compact modeling for circuit simulation also much closer to 2-

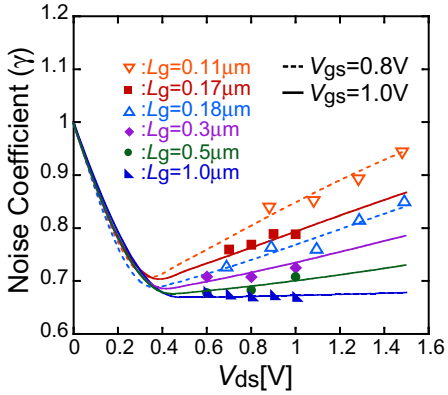

Fig. 8: Calculated thermal noise coefficients γ and measurements as a function of the drain voltage V_{ds} for various gate lengths L_g.

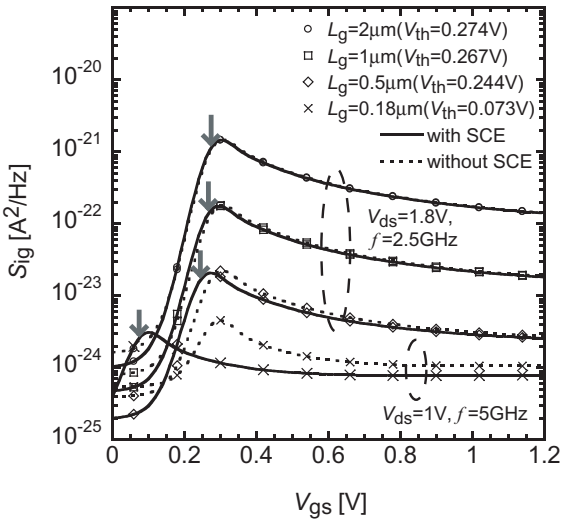

Fig. 9: Comparison of calculated induced-gate noise S_{ig} with the short-channel effect and without. The threshold voltages are depicted by arrows.

dimensional numerical device simulation. Therefore, both approaches can now come together and work united to achieve the common goal of realizing rapid technology progress for the benefit of the society.

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