Silicon Nanowire Transistor Fabrication by the Self-assembling "Grow-in-Place" Approach with Mass Manufacturability

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ABSTRACT

The use of silicon nanowires (SiNWs) in electronic device applications typically uses a grow-and-place approach requiring SiNW growth, harvesting, positioning, and finally device fabrication. The harvesting and positioning steps provide significant impediments to mass manufacturing. To address these problems, we have introduced a novel nanochannel-guided self-assembling "grow-in-place" approach. This methodology uses a horizontal, permanent nanochannel template to guide vapor-liquid-solid (VLS) nanowire growth, and, combined with core-shell top gate geometry, results in SiNW transistor structures without any harvesting and positioning steps.

Keywords: nanowire, transistor, grow-in-place, guiding-nanochannel template, self-assembling, mass manufacturability

INTRODUCTION

One dimensional nanoscale materials, such as nanowires and nanotubes, have attracted much attention as the potential building blocks [1] for emerging nanotechnologies. Among the promising nanowire and nanotube materials, silicon nanowires (SiNWs) appear particularly attractive due to the central role of silicon in the semiconductor industry. Potential applications of SiNWs ranging from nanoelectronics [2,3] to biosensors [4] have been demonstrated.

A number of different methods for synthesizing and assembling SiNWs for device fabrication have been explored. These methods have predominantly used some version of a grow-and-place fabrication methodology, which generally involves the three major steps of SiNW growing, harvesting, and placing (positioning and orienting) followed by device fabrication [5,6,7,8]. In these various methods, the "growing" step is generally based on the vapor-liquid-solid (VLS) catalyst growth mechanism which was first introduced by R. S. Wagner et al [9]. This mechanism offers single crystal SiNWs with good size control since the cross sectional size (e.g., the diameter of the SiNWs) is determined by the size of the catalyst [10]. The "harvesting" step, however, generally results in SiNWs in solution and a "placing" step is required to relocate the SiNW from a solution to locations on a substrate selected for subsequent device fabrication. For SiNWs this "placing" step generally has two common forms: the "surface-patterning fluidic alignment" [11] and "electric-field assembly" [12] methods. In these techniques, the synthesized SiNWs are harvested into solution and sorted for size and length. The sorted SiNWs in the solution are then positioned and aligned through either surface patterning flow or electric fields. Finally the aligned nanowires are fabricated into devices such as transistors. The involvement of nanowire harvesting and placing (positioning and alignment) operations limits device mass-manufacturability and the compatibility with standard semiconductor fabrication. In addition, with the using of surface patterning in the "surface-patterning fluidic alignment" or electrical pads in the "electric-field assembly" approaches, obtaining acceptable inter-device packing for practical applications is difficult. A previous attempt to circumvent these grow-and-place steps is found in the "patterned growth" [13] method. First proposed as a carbon nanotube growth-positioning approach [13,14], it has been used also for Ge NWs [15]. However, the patterned growth method does not give control over the number, direction, or inter-wire spacing of the nanowires produced.

We report here on our efforts to side-step the problems of the various "grow-and-place" approaches and of the "patterned growth" approach to SiNW electronic device fabrication by using a novel nanochannel-template-guided "grow-in-place" [16] methodology. This approach to SiNW device fabrication, which can use various substrates including silicon or glass, is a further development of our "grow-in-place" nanowire growth method introduced earlier [17,18]. In the "grow-in-place" methodology, a horizontal nanochannel template (Fig. 1c, d), positioned at the final location of the required device (in this example, a transistor), is used to "nurse" initial SiNW growth through the VLS mechanism (Fig. 1e). By controlling the growth time and conditions, the nanowire can grow and extrude to the predetermined length (Fig. 1f, Fig. 2). The extruded nanowire is then subjected in situ to device fabrication steps such as thermal oxidation, surface passivation, contact formation, and ion-implantation. Thus, our approach offers nanowire device mass manufacturability.

EXPERIMENT AND RESULTS

To direct and control SiNW growth in the grow-in-place approach, the guiding nanochannel template must first be fabricated on the substrate at the location of the required device. This template can be made by electron-beam lithography or nanoimprinting. Here we used electron-beam lithography following the procedure of our previous work [17,18]. The sacrificial material used in template channel formation was gold allowing it to also serve as the catalyst for VLS SiNW growth. The overall process flow for the guiding nanochannel template is summarized in Fig. 1. First, open trenches (one is shown) of desired size, number, inter-wire spacing, orientation, and location were patterned by electron-beam direct writing on a resist film (PMMA) on a substrate (glass or silicon). Alignment markers were also defined for following capping layer and electrode contact definitions. Second, titanium (1.5nm) was e-gun evaporated as an adhesion layer and then gold was thermally evaporated to a desired nanometer thickness thereby defining the height of the channel (Fig. 1a). Subsequently, the resist film was lifted off to reveal the gold line positioned and spaced, as desired, on the substrate (Fig. 1b). The e-beam writing and Au deposition defined the Au line dimension. Third, a capping layer (e.g., silicon oxide) with the designed width (e.g., 3 μm) was patterned by photolithography, deposition and lift-off (Figure 1c). Finally, the gold line, including the region buried under capping layer, was controllably removed by wet etching to form a channel devoid of Au except for a slug of Au for catalyzing the VLS process, as depicted in Fig 1d. For this gold removal process, a diluted Au etchant (type TFA from Transene Company, Inc.) was employed at room temperature and the etching was stopped by immersion in DI water. The small slug of Au (e.g., sub 1 μm) retained for its catalyst role was located in the middle of the otherwise empty channel (Fig. 1d).

In carrying out our grow-in-place method, the VLS growth was done in an LPCVD reactor at 500 °C and 13 Torr, using 5% SiH_4 diluted in H_2 with a total flow rate of 100 sccm [17,19]. Fig. 1e shows the schematic nanowire growth. The nanochannel template guided the VLS nanowire growth as seen in Fig. 1e resulting in SiNWs. For the growth parameters used, the SiNWs grew out of the guiding nanochannels at a growth rate of 1 μm/min. We allowed the nanowires to grow to a length of 15 μm to permit easy four contact, or gate and source/drain photolithographic definition, depending on whether four probe structures for resistivity-contact resistance studies or transistors were being fabricated. After the nanowire growth, the residual gold was completely removed by rinsing the whole sample in gold etchant following by DI water cleaning. The SiNWs were then subjected to a modified standard cleaning. After these processes, the nanowire as shown in Fig. 1f is ready for device fabrication in its position.

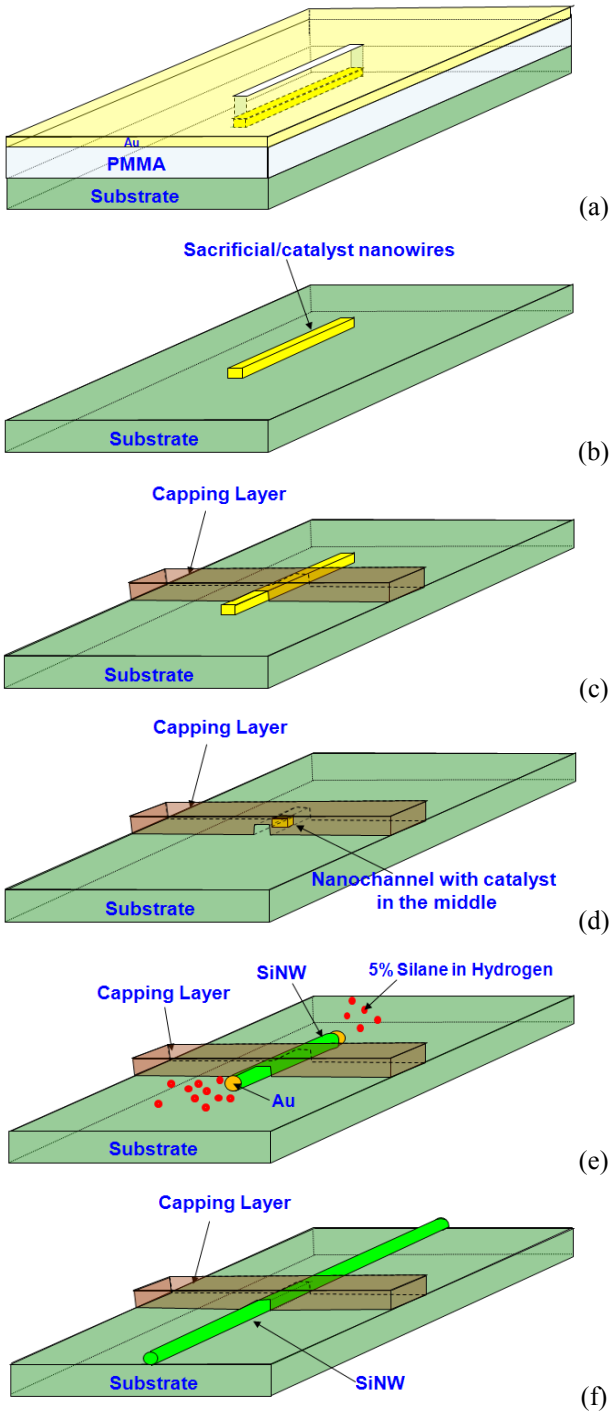

Figure 1. Schematic showing the process flow for one "nursing" nanochannel template fabrication and the SiNW growth from our "grow-in-place" method for device applications. (a) Sacrificial/catalyst metal definition and deposition. (b) Sacrificial/catalyst line after lift-off. (c) Capping layer formation by lithographic patterning, deposition, and lift-off. (d) Partial etching of the sacrificial metal to form the nanochannels with catalyst in the middle. (e) LPCVD SiNW growth and extrusion out of channel by the VLS mechanism. (f) SiNW ready for device fabrication.

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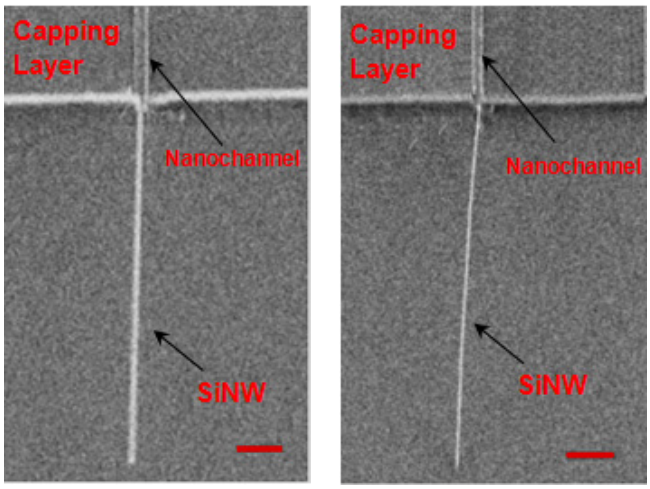
Fig. 2 shows scanning electron microscope (SEM) images of SiNWs growing from different cross-sectional sized nanochannels in this "grow-in-place" approach. Fig. 2a shows SiNW of 150nm in diameter and Fig. 2b shows SiNW of 80nm in diameter. The SEM images clearly show that SiNW grew and extruded from the nanochannel. The pre-fabricated nanochannel defined the SiNW size, position and growth direction. By using alignment markers and the grown SiNW fixed by the nanochannel, a transistor can be easily fabricated from these well controlled, self-positioned "grow-in-place" nanowires.



(a) (b)

Figure 2. SEM images of SiNWs produced by the "grow-in-place" method. Extrusion out of "nursing" nanochannel is evident. (a) 150nm width SiNW, and (b) 80nm width SiNW.

When transistors were fabricated from the grow-in-place SiNW (Fig. 3a), an encapsulating SiO_2 layer was first grown on the wire by dry thermal oxidation [20,21] at 700 ^oC for 4 hours [20,22] using a 3 L/min O_2 flow rate. This oxidation resulted in a Si/SiO_2 core-shell structure [20, 22,23,24] with ~10 nm thermal silicon oxide surrounding the SiNWs (Fig. 3b). This thermal oxide becomes the gate dielectric of transistors and it also serves to passivate the SiNW surface and reduce SiNW surface state density. Second, the top gate electrodes of the SiNW FET structures were then fabricated on these core-shell $SiNW/SiO_2$ structures by spinning on the twin-layer photoresists (LOR5A/SPR3012) and opening up the gate region through photolithography. The gate contacts were formed as shown in Fig. 3b by metals Ti (400nm)/Au (50nm) deposition and lift-off. Third, the source/drain contacts were then fabricated on these core-shell $SiNW/SiO_2$ structures in similar way, but with oxide removal. The twin-layer photoresists (LOR5A/SPR3012) was spun on and the source and drain regions were opened. The photoresist layer in this step served as a mask for etching the silicon oxide as well as defining source/drain contacts. After the silicon oxide surrounding the silicon nanowire in the source/drain

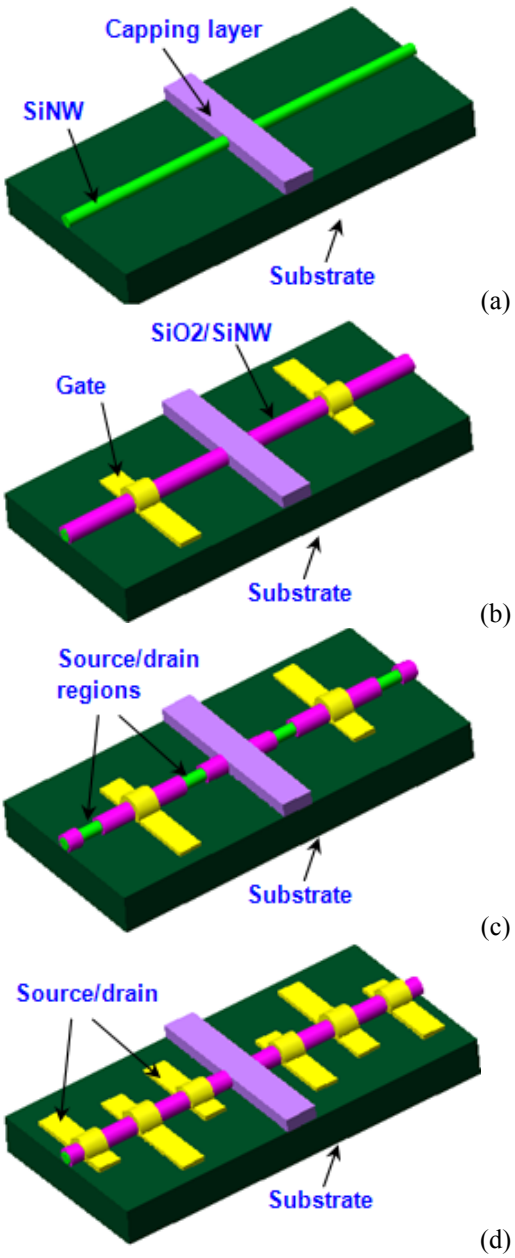


Figure 3. Schematic representations of the top-gate SiNW transistor fabrication process. (a) SiNW after cleaning, (b) SiNW oxidation and gate contact patterning, (c) Source/drain region patterning and oxide removal, (d) Source and drain contact deposition

regions was etched (Fig. 3c), the contact metals (400nm Ti/50nm Au) were deposited with the Ti contacting the SiNW, followed by lift-off (Fig. 3d).

We have successfully made transistors from our "grow-in-place" SiNWs through the process steps summarized in Fig. 3. Using the processing that has been discussed here, a "nursing" nanochannel with a 45nm by 100nm cross-section will result typically in an ~80 nm diameter SiNW transistor structure including its surrounding oxide. We estimate the actual SiNW to have a diameter of ~60 nm and

to have a ~10nm thick oxide shell. Oxides, grown by others, which envelope SiNW in this same manner, have been shown by transmission electron microscopy (TEM) characterization to have very good interface structural quality [20]. From the electrical measurements, our SiNW transistors showed on/off ratios of about six orders of magnitude. The SEM images, electrical measurements, detailed results and discussions will be shown in future publications.

SUMMARY

In summary, our grow-in-place approach offers the ability to synthesize self-positioned/self-assembled SiNWs in place, for SiNW device fabrication, directly from the Si source gas, without any intervening silicon material formation, harvesting, positioning, and assembling steps. A permanent nanochannel in this approach guides the SiNW during VLS nanowire growth and gives control of nanowire size, number, position, orientation and inter-wire spacing. This grow-in-place nanowire device fabrication approach offers the possibility of mass-manufacturably without any "grow-and-place" difficulties. In addition, our nanowire fabrication approach is environmentally benign [25] since the fabricated nanowires are always fixed by the guiding channels and only the exact number of nanowires needed is fabricated.

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