Impact of Gate Induced Drain Leakage and Impact Ionization Currents on Hysteresis Modeling of PD SOI Circuits

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ABSTRACT

The impact of the gate induced drain leakage and impact ionization currents on hysteresis of PD FB SOI circuits is examined, and a physical understanding is provided. Measured silicon data from 90nm and 65nm PD SOI technologies indicate that both components dominate in the substrate currents at zero gate voltage and non-zero drain voltages. Substrate currents under these particular conditions are critical to pre-first-switch body voltage establishment, which is definitively validated by a compact modeling experiment. As the OFF-state channel leakage current increases in scaled technologies, these substrate currents need to be closely monitored and well modeled to properly predict and understand evolution of the hysteresis behavior.

Keywords: compact modeling, GIDL, hysteresis, impact ionization, PD SOI, substrate current

1 INTRODUCTION

The dependence of switch delay of a partially depleted (PD) floating-body (FB) silicon-on-insulator (SOI) circuit on its previous state, known as hysteresis, is caused by the dynamically changing body voltage of PD FB SOI MOSFETs [1]. The body voltage, in turn, is generally determined by capacitive coupling in the drain/body/gate network and secondary parasitic currents. The roles of major parasitic currents in hysteresis, such as forward and reverse diode currents, and gate-to-body tunneling current, have been well explained [1,2]. Their implications to compact modeling and related model optimization methodologies have been studied in depth [3,4,5].

The other parasitic current is the body current, which can be measured in tied-body SOI devices and is the equivalent of the substrate current in bulk technologies (and henceforth it will be referred to as the substrate current). It is generally considered that the substrate current charges the floating body of PD FB SOI devices through the impact ionization process, thus contributing to the hysteresis effect. In Figure 1, a sample simulated hysteresis behavior of a PD FB SOI inverter chain is illustrated, where hysteresis is defined as the percentage difference between propagation delays of the first and second switches of each gate [4]. As the impact ionization current increases (by tuning the BSIM PD/SOI model parameter *alpha0*), hysteresis reduces considerably, particularly in the high supply voltage region. Meanwhile, the output characteristics of PD FB SOI devices are sensitive to the impact ionization current as well. Consequently, appropriate modeling of the substrate current is required. The exact mechanism of the substrate current's influence on hysteresis in PD FB SOI circuits, however, has not been addressed in detail; neither has the corresponding model extraction strategy been studied.

In this paper, a physical understanding of the substrate current's role in hysteresis is provided in Section 2, supported by component analysis of the substrate current in the state-of-the-art 90nm and 65nm PD SOI technologies in Section 3. In Section 4, it is further validated definitively through a compact modeling experiment. Finally, practical guidelines are provided for the substrate current modeling to achieve improved accuracy in modeling of hysteresis as well as devices' output characteristics.

2 PHYSICAL UNDERSTANDING

The switching speed of a PD FB SOI MOSFET is determined by the body voltage immediately prior to the switch through the body sensitivity of threshold voltages. The terminal voltages of an NFET in the inverter configuration prior to its first switch (i.e., pull-down) are illustrated in Figure 2. It has been shown [2,3,4] that the body voltage, which governs the ensuing first switch delay, is given by the KCL balance of the gate-to-body tunneling current in accumulation ($I_{gb,ACC}$), the forward ($I_{j,FWD}$) and reverse ($I_{j,REV}$) diode currents. Generally, $I_{gb,ACC}$ is a few orders of magnitude lower than $I_{j,FWD}$ [4].

A closer look at the bias conditions in the NFET prior to its first switch, however, reveals that there may be two additional current components contributing to the body voltage (Figure 3). First of all, the large drain-to-gate voltage creates condition for the gate induced drain leakage current (GIDL) [6], I_{GIDL}, where the holes flow into the floating body as a result of the band-to-band tunneling of valence-band electrons. Second, impact ionization (II), I_{II}, may take place since a non-zero channel leakage current occurs under the high drain-to-source voltage (i.e., the nominal OFF-state current of the transistor). Consequently, it may become necessary to take into account both I_{GIDL} and I_{II} in the body voltage calculation depending on their strength relative to the reverse diode current $I_{j,REV}$.

The conventional scheme (Figure 4) that explains the DC current balance leading to the body voltage prior to the second switch [4] remains accurate and complete. Lack of the channel current in this case precludes impact ionization. As a result, the above analysis of the MOSFET bias conditions related to the first and second switches indicates that the substrate currents under a single specific circumstance, that is, zero gate voltage (V_{GS}=0), may be critical to hysteresis and its modeling in PD SOI circuits if

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the GIDL and II currents become comparable to or great than the reverse diode current.

3 SILICON DATA ANALYSIS

Component characterization and analysis of the substrate current at zero gate voltage, i.e., the gate-induced drain leakage, impact ionization, and junction leakage currents, can be made possible by combining the electrical test results from three measurement schemes. One of such schemes is shown in Figure 5, where the body voltage sweeps with all other terminals grounded and the drain/source currents are measured. The drain (or source) current so measured represents the clean diode current, as illustrated in Figure 5 for a tied-body PMOS transistor in a 90nm PD SOI technology (the reverse diode current in this particular device happens to be below the instrument's resolution level).

The second measurement scheme is where the drain and source are tied together and sweep in sync while both the gate and body are grounded (Figure 6). The body current in this case represents the sum of the diode currents through the drain-body and source-body junctions except for the high reverse bias region, where additional GIDL current emerges as shown in Figure 6. Side-by-side comparison of the body current in the drain-sweep scheme versus the drain current in the body-sweep scheme provides a quantitative evaluation of the GIDL current (Figure 8).

The final scheme is the regular substrate current measurement setup (Figure 7), where the substrate current vs. gate voltage IV characteristics are obtained for a set of drain voltages. Of particular interest to the hysteresis effect, as explained in Section 2, would be the data points at zero gate voltage (circled in Figure 7). The measurement conditions for these data points differ from the drain-sweep scheme (Figure 6) by a non-zero drain-source voltage. Consequently, overlaying the circled data points with results from previous two measurements reveals the magnitude of the impact ionization current (Figure 8).

As it is clearly seen in Figure 8, the KCL balance that determines the pre-first-switch body voltage is indeed established between the forward diode current and the substrate current (i.e., combination of the GIDL and II currents on top of the reverse diode current) rather than the reverse diode current alone. As the substrate current increases, the increased pre-first-switch body voltage leads to a faster first switch and subsequently lower hysteresis. It is also worth mentioning that the GIDL and II currents at zero gate voltage are of comparable values as illustrated in Figure 9. Similar results are obtained for a 65nm PD SOI technology on an example of an NMOS transistor (Figure 10). The evidence from measured silicon data accentuates the importance of proper modeling of the substrate currents at zero gate voltage.

4 MODELING EXPERIMENT

A modeling experiment is designed and carried out to further confirm and isolate the impact of substrate current on hysteresis. In the experiment, the same NMOS model card is used with three slightly different PMOS model cards to simulate the hysteresis of an inverter chain. It is verified that the substrate currents at V_{GS}=0V in the base PMOS model are noticeably larger than the reverse diode current, as in the cases demonstrated in Section 3. Compared with the base PMOS model, the second PMOS model has an overall elevated substrate current by 10x as measured at V_{GS}=0.7V and V_{DS}=1.4V (by tuning model parameter *alpha0*). And the third model has a 'tilted' substrate current, which is almost identical to the base model at V_{GS}=0V whereas being elevated by 10x at V_{GS}=0.7V and V_{DS}=1.4V (by tuning model parameters *alpha0*, *vdsatii0*, *sii0*), as illustrated in Figure 11.

SPICE simulations, given in Figure 12, show that the model with 10x elevated substrate current noticeably reduces hysteresis at high voltages with respect to the base model, as fully expected,. The base model and the 'tilted' model, however, produce nearly identical hysteresis. It definitively confirms the physical understanding of the impact of the substrate current on hysteresis given in Section 2, and particularly the fact that such an impact solely comes from the substrate currents specifically measured at zero gate voltage.

The findings indicate that, whereas the substrate current modeling, mainly through its impact ionization component, can sometimes be used for output characteristics modeling optimization, it is critical to maintain a good model-to-data fit at zero gate voltage to ensure accuracy in hysteresis modeling. In addition, as devices scale or threshold voltage reduces, the substrate current at zero gate voltage needs to be closely monitored, because of increased channel leakage current, to properly predict and understand the evolution of hysteresis behavior.

5 CONCLUSIONS

The impact of the GIDL and impact ionization currents, two major components of the substrate current, on hysteresis of PD FB SOI circuits is examined, and a physical understanding is provided that substrate currents at zero gate voltage are critical to the pre-first-switch body voltage establishment, and consequently, to hysteresis. It is supported by measured silicon data from 90nm and 65nm PD SOI technologies as well as a modeling experiment. As the OFF-state channel leakage current increases in scaled technologies, substrate currents at zero gate voltage need to be closely monitored and well modeled to properly predict and understand the evolution of hysteresis behavior.

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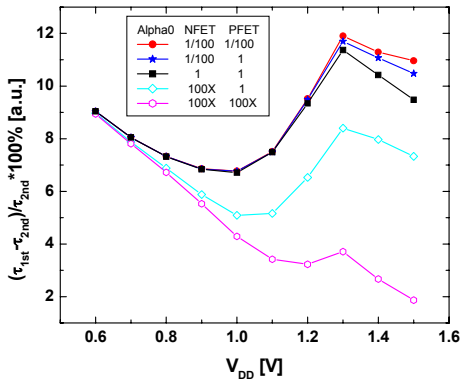

Figure 1 Illustration of the impact ionization current's influence on hysteresis (V_{DD}: supply voltage)

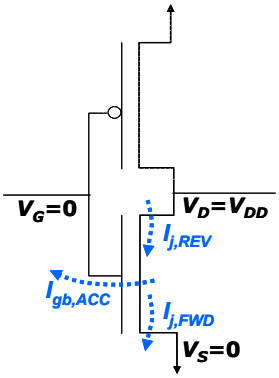

Figure 2 Terminal voltages for NFET in an inverter configuration prior to the first switch, and parasitic currents that determine the body voltage [4]

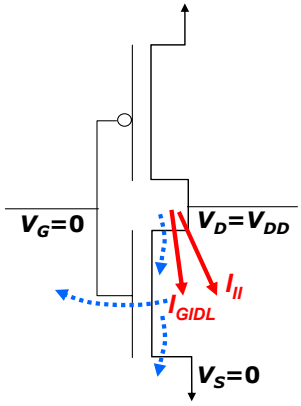

Figure 3 Contribution of the GIDL current and impact ionization current to the body voltage prior to the first switch

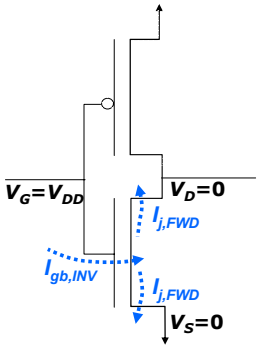

Figure 4 Terminal voltages for NFET in an inverter configuration prior to the second switch, and parasitic currents that, along with the subsequent drain-body capacitive coupling, determine the body voltage [4]

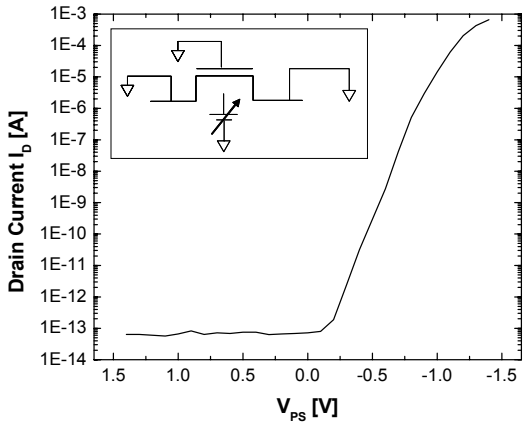

Figure 5 Diode current in a 90nm tied-body PD SOI PMOS transistor (inset: measurement setup)

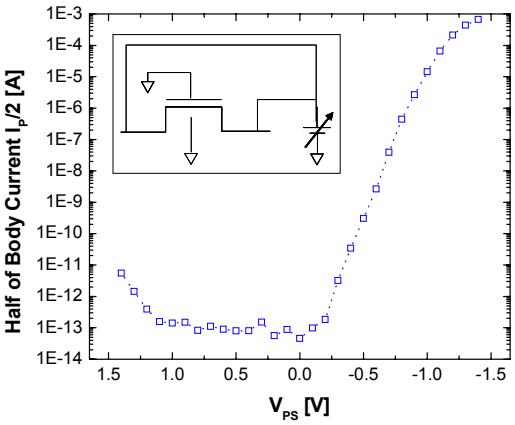

Figure 6 Diode and GIDL currents in a 90nm tied-body PD SOI PMOS transistor (inset: measurement setup)

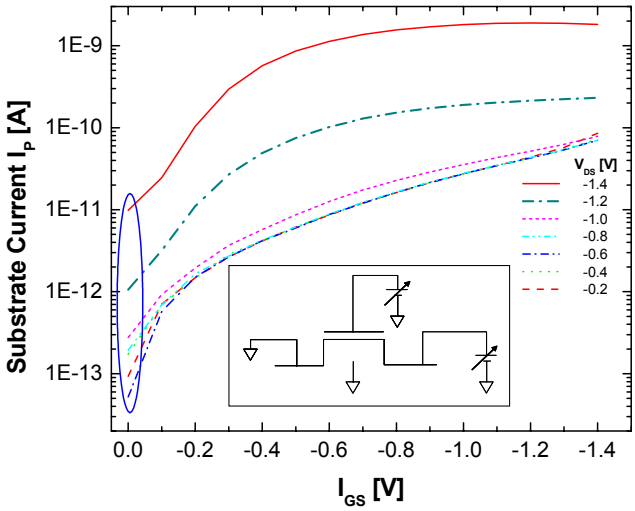

Figure 7 Substrate current in a 90nm tied-body PD SOI PMOS transistor (inset: measurement setup)

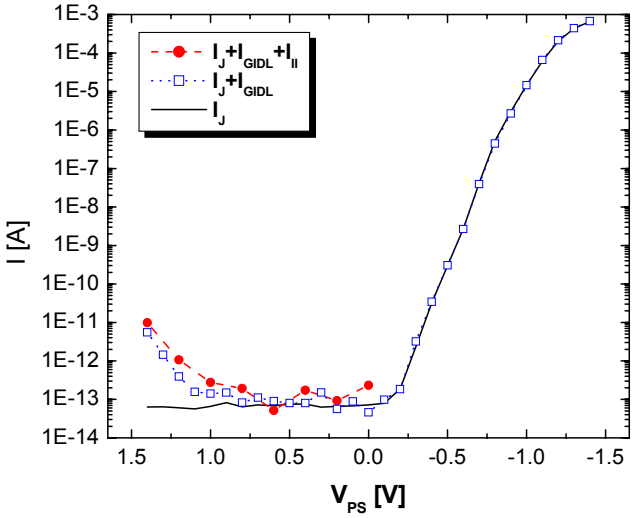

Figure 8 Components of substrate current vs. forward diode current in a 90nm tied-body PD SOI PMOS transistor

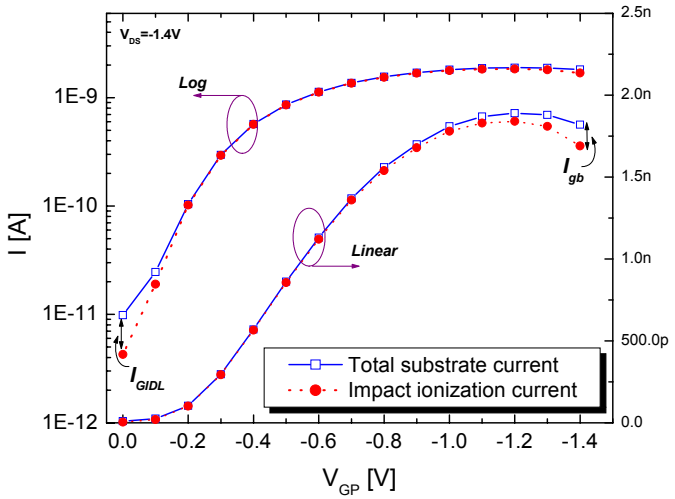

Figure 9 Impact ionization current vs. total substrate current

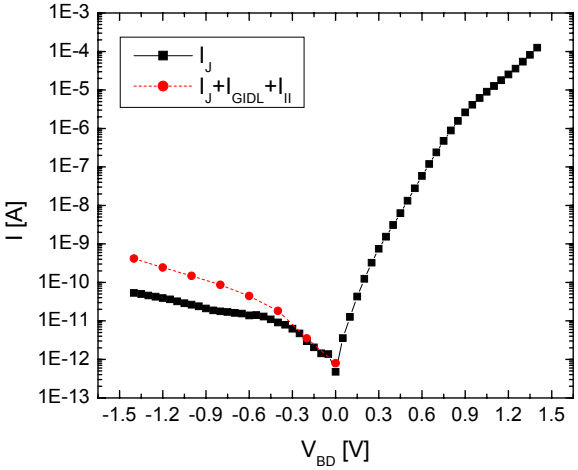

Figure 10 Components of substrate current vs. forward diode current in a 65nm tied-body PD SOI NMOS transistor

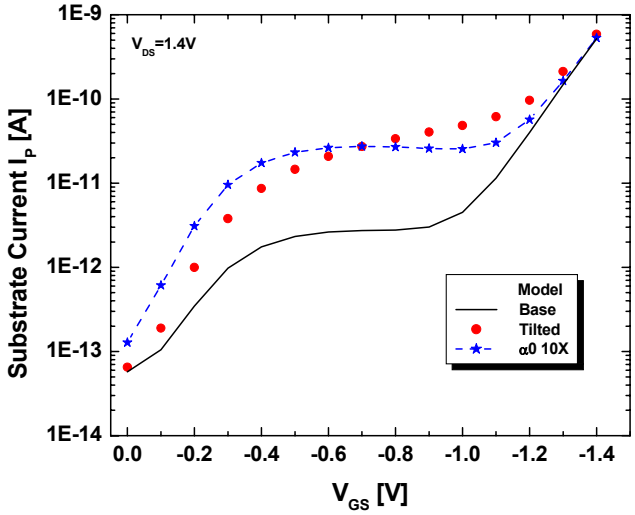

Figure 11 Substrate current behavior of three BSIM PD/SOI models under test

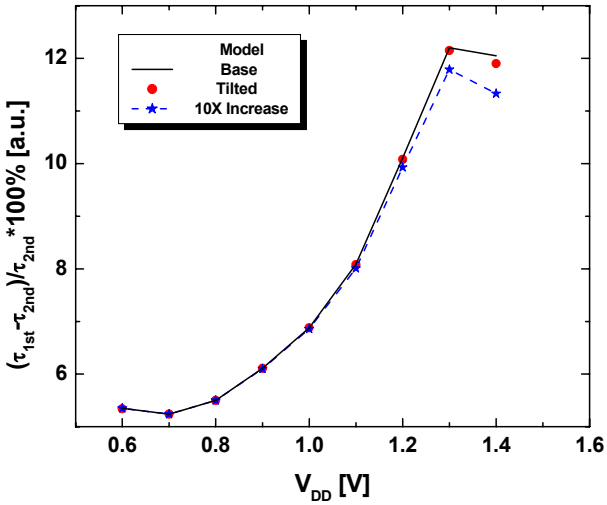

Figure 12 Hysteresis behavior comparison for three BSIM PD/SOI models under test