1/f Noise and RTS(Random Telegraph Signal) Errors in Comparators and Sense Amplifiers

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ABSTRACT

Noise signals can be equivalently represented in either the frequency domain or the time domain. The representation or modeling in the frequency domain gives the mean square noise current of a transistor as a function of frequency. The representation or modeling of the RTS or l/f noise of nanoscale devices that is easiest to understand is that done in the time domain. The capture and emission of a single electron in a nanoscale NMOS transistor with be equivalent to a change in threshold voltage. Modern devices are now small enough that we can see RTS noise signals associated with single electron trapping. These changes in threshold voltage result in a mismatch in comparators and sense amplifiers in CMOS integrated circuits,

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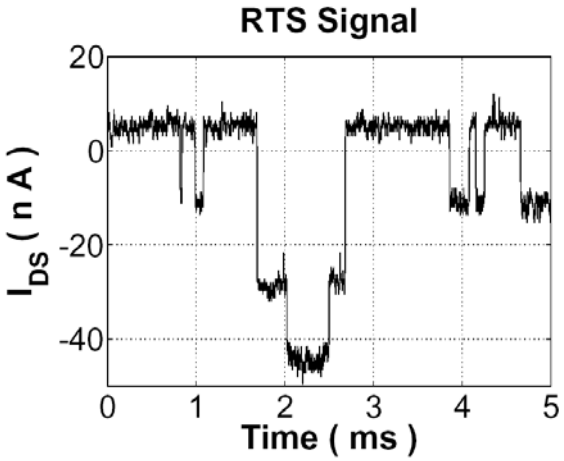

Fig. 1 RTS noise due to trapping and emission of a multiple electrons in a nanoscale n-channel CMOS transistor. This is the representation in the time domain over millisecond time periods of l/f noise, this and other signals with many different capture and emission times will combine and result in l/f noise in the frequency domain. The noise in the frequency domain will be characterized by a noise parameter value KF.

1 INTRODUCTION

An analysis has previously been made of the increasing portion of the threshold voltage being occupied by thermal noise levels and the bit error rates in digital logic[1] and memory circuits [2-4]. This analysis has led to the prediction that there are fundamental limits imposed in digital circuits by thermal noise and that the scaling predicted by Moore's law can not continue into the future.[1] No consideration was, however, given to the errors that might be caused by l/f noise or random telegraph signals. In small transistors such as used in read sense amplifiers the l/f noise is caused by and can be characterized by random telegraph signals(RTS), Fig. 1. These random signals can cause errors in the sense amplifiers and limit the ability to read the data stored in memories.

2 RTS NOISE

These noise signals can be equivalently represented in either the frequency domain or the time domain. The representation or modeling in the frequency domain, using the NLEV=0 SPICE

noise model, gives the mean square noise current of the read transistor is

$$I^2 = KF\ \mu\ W\ (Vgs-Vt)^2 / (2\ L^3\ f) \quad (1)$$

where, KF is the l/f noise parameter, L the length and W the width of the transistor channel, μ the mobility and (Vgs-Vt) the excess of gate voltage above threshold. The voltage read error of a sense amplifier transistor can be expressed as

$$\Delta V = \Delta I\ \Delta t / Cbit \quad (2)$$

$$\Delta V = ((KF\ W\ \mu / 2\ L^3)\ (\ln (fh/fl))\ )^{1/2} (Vgs-Vt)\ \Delta t / Cbit \quad (3)$$

where, fl and fh are the low and high frequency bandwidth limits. Δt is the read interval or access time of the signal at the sense amplifier and Cbit the bit or data line capacitance. This average or mean error signal will be small of the order millivolts. This however is the mean read error voltage, there is a small but finite probability of much larger read errors, such as tens of millivolts, in the same sense there is a small but finite probability of large errors to due to thermal noise.

In the case of RTS and l/f noise in the time domain representation the small but finite probability of an error will result from all traps happening to capture or emit electrons at the same time. If all traps in the sense amplifier transistor capture or emit electrons at the same time there will be an erroneous sense amplifier signal, the probability of such an error is small but it will occur at random times. This will result in an error or give the appearance of there being a "variable retention time" in a particular memory cell. The representation or modeling of the RTS or l/f noise of nanoscale devices that is easiest to understand is that done in the time domain. The capture and emission of a single electron in a nanoscale NMOS transistor of size W/L with be equivalent to a change in threshold voltage, VT, of

$$\Delta VT = q / (Cox\ W\ L) \quad (4)$$

where q is the electronic charge, and Cox is the gate capacitance.

The probability that there will be a coincidence of occurrence of a number of electrons contributing to a large change in threshold voltage and causing an error has been found to be described by a lognormal distribution. In a lognormal distribution the probability of a large value is of the order exp(-x). The published results in Fig. 2 show a 0.1% probability of a value twenty times the minimal

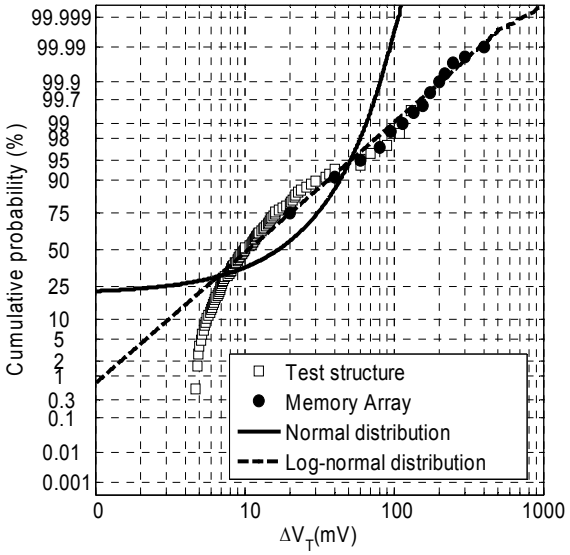

Fig. 2 Threshold voltage distributions on a 90nm transistor with a 9nm gate oxide.[5]

RTS step of 10mV on a minimum size device in a 90nm technology with 9nm gate oxides.[5] This would be 200mV, corresponding to eighty traps changing charge state. For a sense amplifier in 50nm technology with 2nm gate oxides and a transistor size of W/L = 2.5 μm /0.05 μm this translates into a threshold voltage distribution as shown in Fig. 3 if we assume the l/f noise varies according to the NLEV=0 SPICE model.

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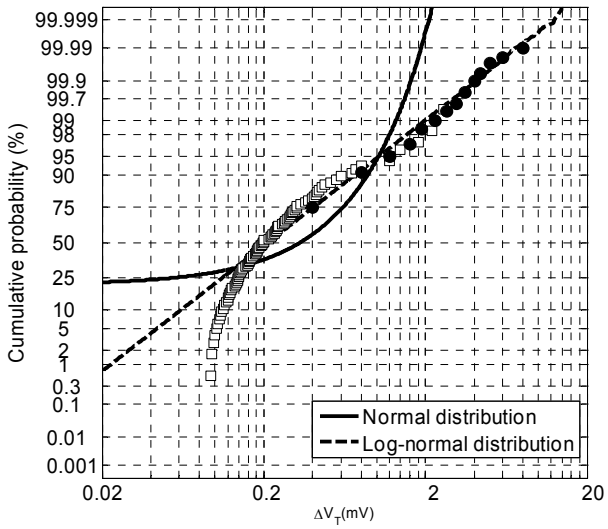

Fig. 3 Calculated threshold voltage distributions on a 50nm transistor with a 2nm gate oxide and gate width, W=2500 nm or W=2.5 μm, a very wide device.

3 CIRCUIT SIMULATION

Fig. 4 shows a simplified representation of a sense amplifier in a dynamic random access memory. The charge stored on the storage capacitor is discharged on to the bit or data line when the word or address line is activated. This causes a signal to be applied to the cross coupled sense amplifier.

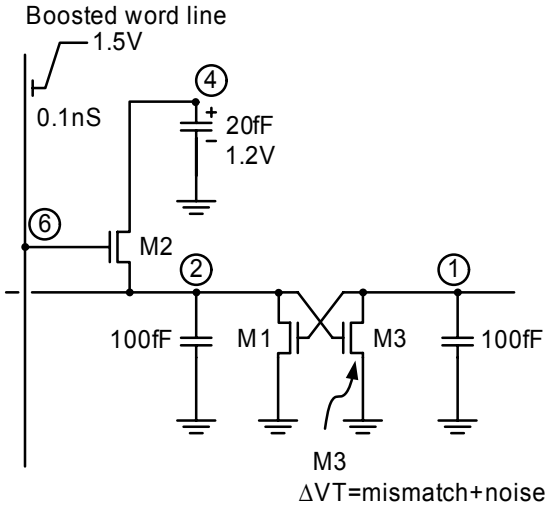

Fig. 4 Circuit diagram of a simplified sense amplifier.

This signal appears as a differential signal and causes an imbalance in the sense amplifier which is amplified as shown by the SPICE circuit simulation in Fig. 5.

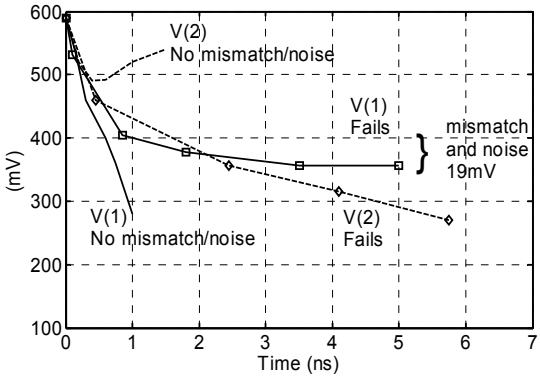

Fig. 5 SPICE simulation showing the effect of offset in a sense amplifier.

RTS noise signals also, however, appear as an offset causing an imbalance in the sense amplifier. If these two signals have opposite polarities than the noise signal can be dominant causing an upset of the sense amplifier and erroneous output. Fig. 6 illustrates the sensitivity of the sense amplifier to noise signals and gives the change in threshold voltage caused by noise which will upset the sense amplifier causing an error [6-8].

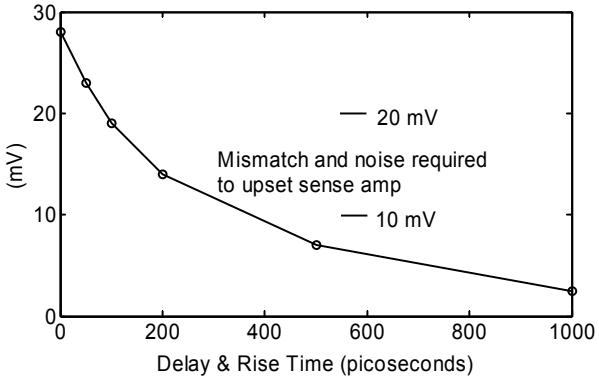

Fig. 6 Sense amplifier upset versus timing.

The sensitivity of the sense amplifier is effected by the time delay over which the noise has had an opportunity to determine the output state or the time before the desired signal is applied by addressing the storage capacitor. A representative value in Fig. 6 is that about a 20 mV threshold voltage offset is sufficient to cause an error if this delay is 100 ps.

Fig. 3 shows there is about a 0.001% probability, or 10^{-5} probability of a 8mV threshold shift in the transistors due to RTS noise. A 20mV threshold voltage shift will occur with a probability of about 10^{-11}. This is still a high error rate for memories so that a proper design would require larger device widths to reduce the error rate. Similar calculations can be made for other device sizes or width to length ratios.

If a DRAM sense amplifier is upset by a threshold voltage mismatch of ΔVT then Fig. 7 shows the calculated error rate.

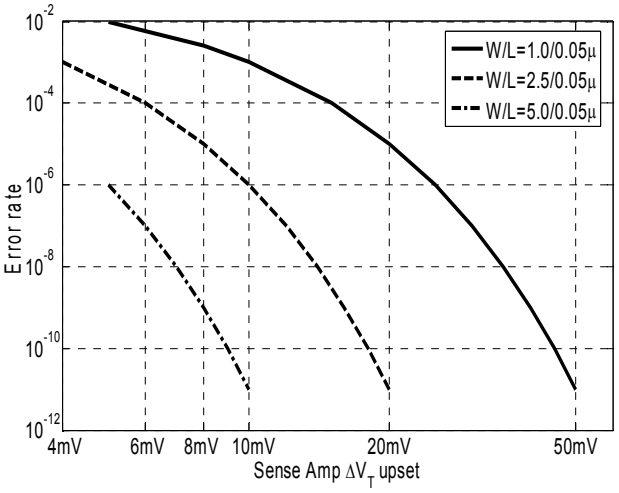

Fig. 7 Error rate on a DRAM sense amplifier due to upset by VT mismatch for different W/L values.

4 CONCLUSIONS

In reality there may not be an error or variable retention time in the memory cell but rather a random and variable error occurring in the sense amplifier due to RTS or l/f noise. This could happen as often as every time a Gbit DRAM is read without proper design and consideration of RTS noise.

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