A New Grounded Lamination Gate (GLG) SOI MOSFET for Diminished Fringe Capacitance Effects

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ABSTRACT

A new Grounded Lamination Gate (GLG) structure is proposed in which grounded metal film is deposited in the spacer region on both sides of the gate to prevent the fringing field lines emanating from the bottom of the gate electrode from entering the source/drain regions. The variation of threshold voltage with gate dielectric permittivity is obtained for both the GLG and the conventional SOI MOSFETs using MEDICI. We demonstrate that the application of grounded lamination gate (GLG) structure is very effective in controlling the threshold voltage roll-off even for high gate dielectric permittivities.

Keywords: silicon-on-insulator MOSFET, high-k gate dielectric, internal fringe capacitance, threshold voltage

1 INTRODUCTION

In highly scaled down MOSFETs using high-K dielectrics, the device gate length may become comparable to the dielectric thickness. As a result, the parasitic capacitance due to the fringing fields from the gate the source/drain becomes an appreciable part of the active device capacitance[1-3]. This will seriously affect the short-channel performance [4-8] of the device due to the undesirable decrease in the threshold voltage with increasing gate dielectric permittivity. It is the purpose of this brief to propose a modification in the SOI-MOSFET structure in order to counter this effect of internal fringe capacitance (C_{bootom}). Grounded metal plates have been introduced in the spacer region on either side of the gate to prevent the fringing field lines emanating from the bottom of the gate electrode from entering the source / drain regions. The characteristics of the new structure are simulated using 2-D device simulator MEDICI [9]. The variation of threshold voltage with gate dielectric permittivity is obtained for both modified and conventional structures. The variation of surface potential along the channel for the two structures is also compared.

2 PROPOSED DEVICE STRUCTURE

A schematic cross-sectional view of the proposed GLG SOI MOSFET structure with high-K gate dielectric is shown in Figure 1, with metal plates of thickness t_p in the spacer region at a distance of t_m from the gate on either side. These metal plates are grounded so that the fringing field lines terminate on these plates rather than the source / drain regions which are at a higher potential. These plates are "buried" in the spacer oxide i.e. they are not in contact with any other part of the device. The plates are a few nanometers above the source/drain region.

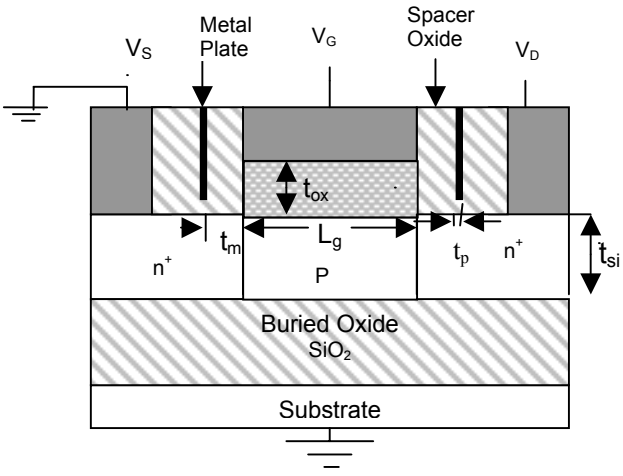

Figure 1: Cross-sectional view of the GLG SOI MOSFET

The distance t_m is optimised for best performance of the device. It is observed that if the plates are too close to the gate (i.e t_m is low) , the gate-to-channel capacitance(C_{ox}) itself gets reduced due to diversion of electric field lines (from the gate electrode to the channel region), responsible for causing inversion, to the grounded metal plates. This results in a very high threshold voltage and very low transconductance. On the other hand, if the plates are too close to the source/drain electrodes (i.e. t_m is large), the external parasitic capacitance become very high resulting in a huge electric field in the spacer region near the metal plates. Also the effectiveness of the metal plates to mitigate the effect of parastic internal fringe capacitance is reduced. For gate length (L_g) of 100 nm and spacer width (t) of 50 nm, the optimum distance of the plates from the gate(t_m) is found to be about 20 nm. The thickness of the metal plates (t_p) is kept small in comparison to the spacer width (for t = 50 nm, t_p = 2-5 nm).

3 DEVICE FABRICATION

The GLG MOSFET can be fabricated using standard CMOS steps as shown in Figure 2. We begin with the MOS structure as shown in Figure 2(a) with the poly gate over the gate dielectric with appropriate equivalent oxide thickness (EOT). In Figure 2(b), a thin SiN layer followed by a TiN layer is deposited using CVD or sputtering each layer having a thickness of about 10-20 nm. A CVD oxide is next deposited and etched using RIE resulting in a sidewall oxide layer as shown in Figure 2(c). A thick dielectric layer using TEOS is deposited and is etched using CMP resulting in the final structure shown in Figure 2(d). The source and drain contacts are made by opening a contact window in the TEOS oxide. After gate, source and drain metallization, we get the GLG MOSFET structure shown in Figure 3.

4 RESULTS AND DISCUSSIONS

The simulation parameters used in the 2-D device simulator MEDICI [9] are shown in Table 1.

Parameter	Value
Source/Drain doping	$2x10^{20}$ cm^{-3}
Channel doping	$3.5x10^{17}$ cm^{-3}
Gate Length (L_g)	100 nm
Distance b/w metal plates & gate (t_m)	20 nm
Thickness of metal plate (t_p)	5 nm
Effective Oxide Thickness (EOT)	2.8 nm
Work Function of gate material	4.35 V
Silicon film thickness	50 nm
Spacer oxide thickness	50 nm
BOX thickness	250 nm
Substrate Thickness	250 nm
Gate electrode thickness	50 nm
Source/drain – Gate overlap	5 nm

Table 1: Simulation Parameters

Figure 4 shows the variation of surface potential along the channel for the conventional and GLG (t_m = 20 nm) SOI MOSFET structures for a gate dielectric permittivity ε_{ox} = 80 and EOT = 2.8 nm. It can be seen that the surface potential is lower for the structure with metal plates. In conventional high-K dielectric SOI MOSFETs, the fringing electric field lines between the gate to the n+ source/drain induce positive charges in the n+ S/D regions [10]. This results in an increase in potential along the channel. However in the GLG structure, the fringing field lines terminate on the metal plates and the effect of the internal fringe capacitance is mitigated leading to a lower surface potential, as evident in Figure 4. The minimum of the surface potential is also lower for the proposed GLG structure, suggesting a later onset of inversion and hence higher threshold voltage.

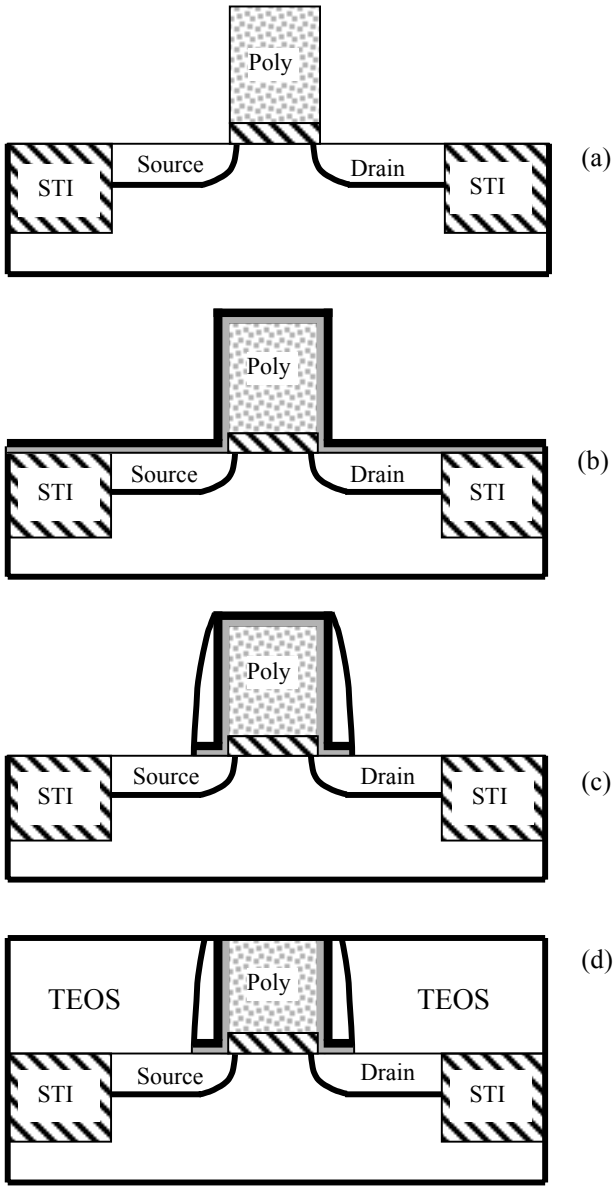

Figure 2: Device fabrication steps (process sequence) for the GLG-MOSFET

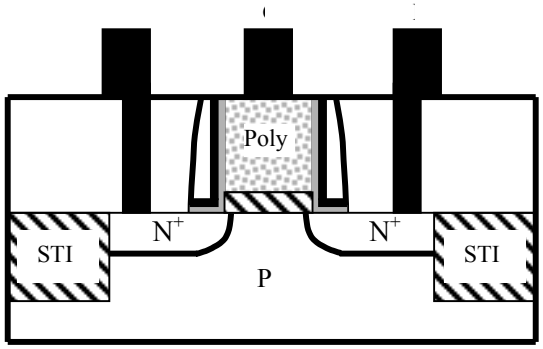

Figure 3: Cross-section of the Grounded Lamination Gate (GLG) MOSFET

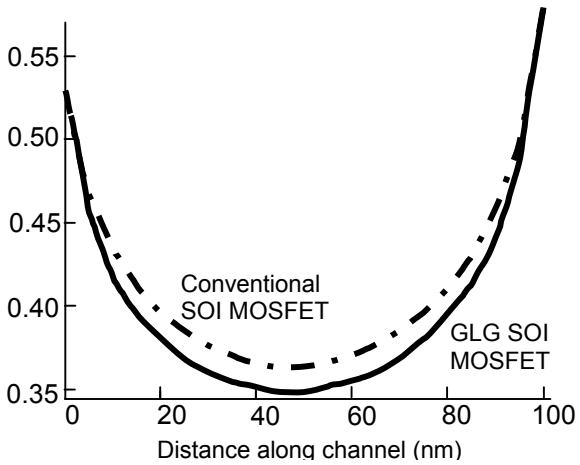

Figure 4: Surface potential variation along the Channel (V_{GS} = 0.02 V, V_{DS} = 0.05 V)

Figure 5 shows the variation of threshold voltage with gate dielectric permittivity for both the structures. It is evident from the figure that the drop in threshold voltage for the structure without metal plates is as high as about 40 mV as gate dielectric permittivity (ε_{ox}) increases from 3.9 to 100. However, for the proposed GLG SOI MOSFET structure, there is a minimal variation in the threshold voltage. For t_m = 20 nm, the threshold voltage is almost constant for the entire range of ε_{ox} with a maximum deviation of as little as 5 mV.

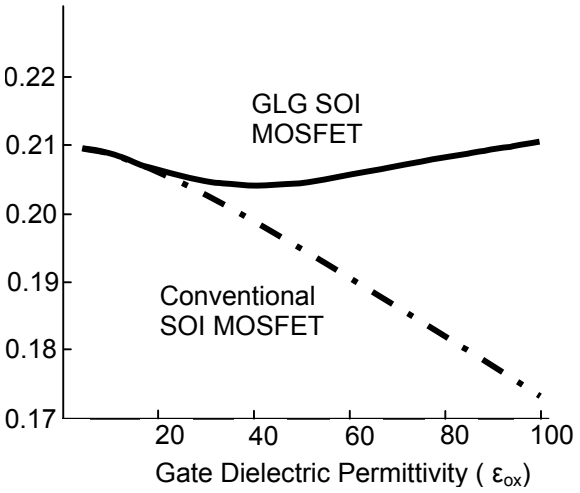

Figure 3: Threshold voltage variation with gate dielectric constant

5 CONCLUSIONS

Proper consideration of fringing capacitance effects is crucial in design and analysis of small geometry high-K gate dielectric SOI-MOSFETs. Using two-dimensional simulation, for the first time, we have presented a new method to effectively extenuate the threshold voltage roll-off with increase in gate dielectric constant (and thus physical gate dielectric thickness) due to parasitic internal fringe capacitance. The proposed structure is expected to be very effective in reducing the fringing capacitance effects which is crucial in the design of high speed small geometry high-K gate dielectric SOI-MOSFETs. The GLG SOI MOSFET can be fabricated using standard CMOS steps. The metal plates should be of appropriately small thickness and need to be placed accurately at the optimum distance from the gate and source/drain regions for effective operation of device.

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