III-V semiconductor nanowires grown on silicon for vertical devices

A. Helman, M. Borgström, O.Wunnicke, W. van den Einden, M. A. Verheijen, A. L. Roest and E. P.A. M. Bakkers

Research Laboratories, Prof. Holstlaan 4, 5656 AE Eindhoven, The Netherlands

ABSTRACT

In this work we explore the potential of III-V semiconductor nanowires grown on silicon for the fabrication of electronic devices such as bipolar and field effect transistors. The main interest arises from the combination of (opto)electronic properties of III-V semiconductors with the existing silicon-based technology. A detailed structural characterization of III-V nanowires grown by laser ablation and metal-organic vapor-phase-epitaxy on silicon has been carried out by means of scanning electron microscopy (SEM) and transmission electron microscopy (TEM) in order to asses the epitaxial growth and the quality of the heterointerface. GaP/GaAs heterostructures and core/shell structures have also been investigated. Electrical characterization is carried out in order to determine transport properties and deduce information about the band structure of the nanowires.

Keywords: nanowires, heteroepitaxy, III-V, silicon, vapor-liquid-solid

1 INTRODUCTION

High-speed operation in silicon devices has been achieved by reducing the device dimensions [1]. Still, some fundamental materials properties such as the indirect band-gap and the mobility limit the performance of silicon based devices. The III-V materials (GaAs, InP, InAs) and their ternary alloys) offer higher mobilities and a direct band gap enabling the fabrication of optoelectronic devices such as LEDs and lasers. Silicon-based technology still has a huge advantage over the III-V's in terms of costs and availability and a significant advancement would be achieved only by the monolithic integration of III-V's with silicon. The heteroepitaxial growth of III-V thin films on silicon has been achieved, but the crystalline quality of the resulting materials is strongly affected by the lattice and thermal expansion coefficient mismatch as well as the formation of antiphase domains due to the growth of a polar material on a non polar substrate [2,3]. The use of nanowires could overcome this problem because of the small contact area between the III-V and the silicon substrate. In this case, the strain at the heterointerface can be accommodated at the nanowire surface without forming dislocations. Antiphase domains are also avoided since a wire grows from only one nucleation site. Recently III-V nanowires have been grown on Si and Ge substrates [4,5]. In this work we present a detailed study of the growth and crystallographic quality of III-V nanowires on silicon with an electrical characterization of the heterointerface.

2 EXPERIMENTAL

Nanowires were grown with the Vapor-Liquid-Solid (VLS) growth mechanism [6] where Au was used as the catalyst. Prior to the deposition of a thin Au film, the oxide on the silicon wafers was removed with a buffered hyfrofluoric acid (BHF) etch. It is known that Au catalyses the oxidation of Si [7], and tens of nm of SiO_2 are formed on top of the gold at room temperature within a period of days. Therefore, the silicon oxide on top of the gold was removed with BHF just before growth. Alternatively, Au colloids with a mean diameter of 20 nm were spincoated on the cleaned and etched Si substrates.

The laser-ablation (LA) set-up used is similar to the one reported in a previous work [8]. The beam of an ArF laser (λ=193 nm, 70 mJ/pulse, 2 Hz) is focused on a pressed III-V target (density 65%). The composition of the wires is, in principle, determined by the composition of the target. The silicon substrate temperature was in the range of 500 to 550°C depending on the choice of the material and an Ar background pressure of 140 mbar was used.

A number of nanowire samples was grown by MetallOrganic Vapor Phase Epitaxy in a Aixtron 200 reactor using trimethylgallium (TMG), trimethylindium (TMI), PH_3 and AsH_3 as precursors in H_2 at a total pressure of 50 mbar in a total flow of 6.0 l/min (slm). The TMG and TMI molar fractions were in the range of 1.5×10^{-5} to 1.5×10^{-4}, and the PH_3 and AsH_3 molar fractions were varied in the range of 7.5×10^{-4} to 5.2×10^{-2}. During heating of the substrate a group V pressure was applied, and when the desired growth temperature was reached, growth was initiated by opening the group III source.

For the characterization of the nanowires on silicon substrates scanning electron microscopy (SEM), transmission electron microscopy (TEM) and X-ray diffraction were used. The samples for the cross sectional TEM were prepared by embedding the wires in 500 nm of SiO_2 by plasma-enhanced chemical vapor deposition. A focused-ion-beam (FIB) was used to cut and lift-out the sample slice. Additionally, the samples were treated with low angle, argon ion milling thinning steps to obtain slices that were thin enough for the high-resoluton TEM studies.

For two terminal electrical measurements InP nanowires, grown epitaxially on silicon, were embedded in a 500 nm-thick poly-methylmethacrylate (PMMA) layer. After the PMMA was spun on, the sample was etched by

reactive ion etching (RIE with O_2) such that the tops of the wires were exposed. For n-InP wires a Ti/Al contact and for p-InP a Ti/Zn/Au top contact was evaporated through a shadow mask. The contact pad sizes were 150×150 μm^2, 100×100 μm^2 and 50×50 μm^2.

3 STRUCTURAL CHARACTERIZATION

In Figure 1 we show a TEM image of a GaP wire grown by laser ablation on a Si (111) substrate. The wire has grown perpendicular to the substrate and extends along the <111> direction. The typical dimensions are 180 nm for the diameter and 2 μm for the length, which appears uniform within the samples. The diameter is also constant along the wire, except for a short thickening at the base. Metal particles are found at the top of all the wires but some of them are also found on the substrate surface.

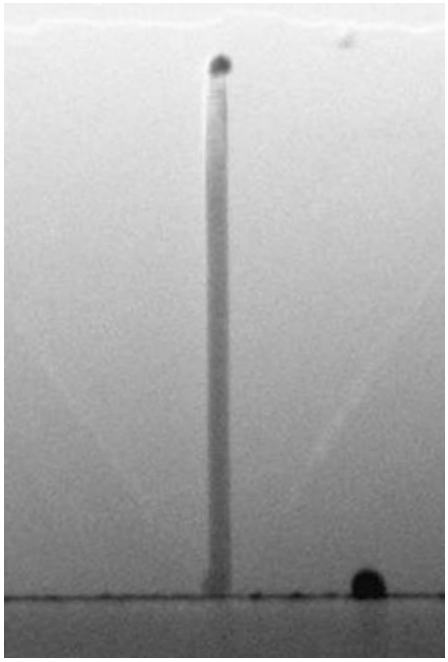

Figure 1: Cross-section TEM image of a GaP wire on a Si (111) substrate.

The high resolution TEM image of the heterointerface between the III-V wire and the silicon substrate is shown in Figure 2. The crystal planes continue from the Si substrate into the GaP wire, confirming epitaxial growth. However, this interface is not atomically flat and the estimated roughness is between 5-10 nm. We believe that this roughness is due to the formation of a Si/Au eutect prior to the nanowire growth. Separate studies of the evolution of the Au/silicon surface at 525°C under argon flow but without ablating from the target, have shown that the Au particles partly consume the Si substrate thus exposing the {111} facets. Once the III-V growth is initiated, the alloyed silicon is excreted giving rise to a rough interface.

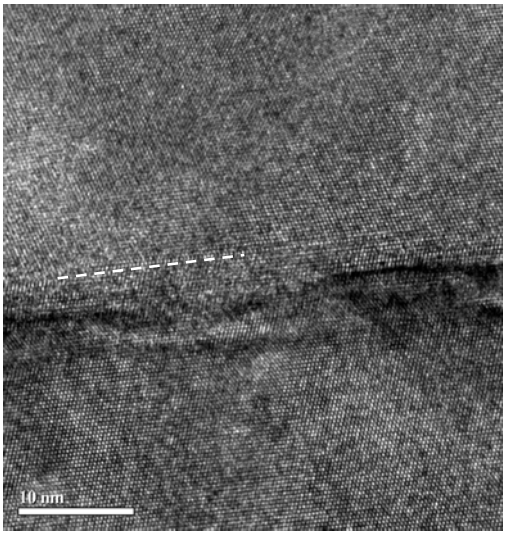

Figure 2: High-resolution TEM image of the GaP/Si heterointerface.

A twin dislocation situated a few nanometers above the heterointerface is indicated by a white dotter line. Twin boundaries can be located in the GaP wires, as in this case, or at the GaP/Si interface.

InP nanowires grown on silicon by MOVPE are shown in Figure 3. The top view SEM image shows wires grown along the four equivalent <111> directions: one perpendicular to the surface (which appear as small bright spots on this image) and three at 120° with respect to each other forming an angle of 19° with the surface. In this case the large number of wires, which are not grown perpendicularly to the surface, can also be explained by the formation of {111} facets prior to the growth. A similar mechanism was proposed for the growth of non-vertical InP nanowires on an InP (001) substrate [9].

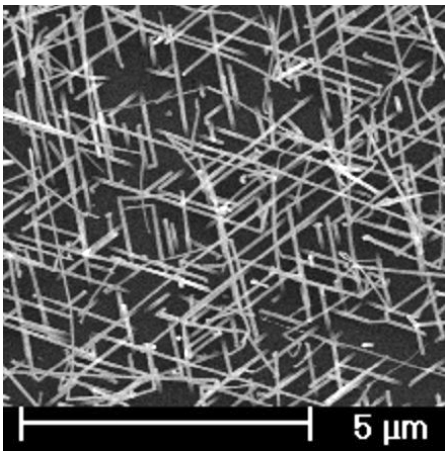

Figure 3: Top view SEM image of InP nanowires grown on a Si (111) substrate by MOVPE.

GaAs wires with a controlled position were grown by MOVPE on an e-beam patterned substrate as shown in Figure 5. The thickness of the Au film, the Au dot size and the pitch were 1 nm, 50 nm and 750 nm.

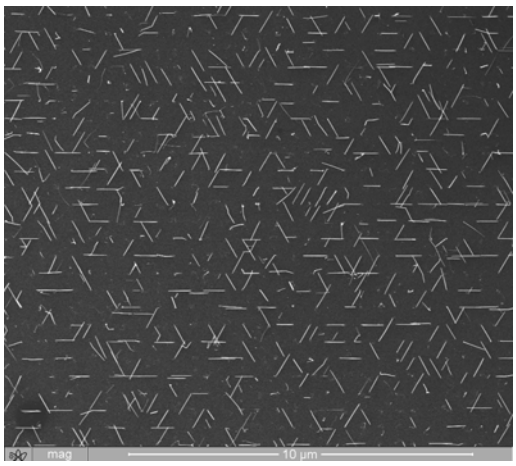

Figure 4: Top view SEM image of GaAs nanowires grown on an e-beam patterned Si (111) substrate by MOVPE.

The observed three-fold symmetry arises from the epitaxial growth along the three <111> directions which are not perpendicular to the surface. The number of vertically grown wires is rather small for this sample.

More complex structures including segmented heterostructures within a nanowire have been grown by MOVPE at 420ºC. In the Figure 5 we show a GaP/GaAs heterostructure with several GaAs segments of different lengths obtained by varying the GaAs growth time [10]. The GaP segments show a high density of twin defects, while the GaAs parts are defect-free. The GaAs grown on GaP shows very sharp interfaces, while GaP on GaAs has a more gradual profile.

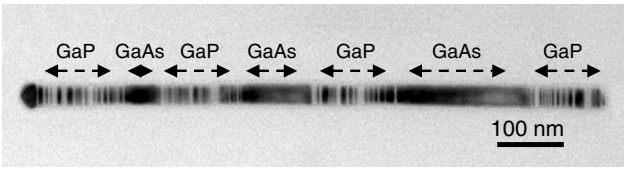

Figure 5: Bright-field TEM image of a GaP/GaAs heterostructure within a nanowire.

For higher growth temperatures (480ºC) the layer growth contribution increases and epitaxial growth occurs at the side facets of the wires as shown in the High Angle Annular Dark Field (HAADF) image in Figure 6. The cross-section of the wire exhibits {211} side facets for the <111> growth direction. The contrast is due to the composition and the dark (bright) regions correspond to GaP (GaAs). From this image we estimate the lateral growth rate to be 0.03nm/s for GaP and 0.17 nm/s for GaAs respectively.

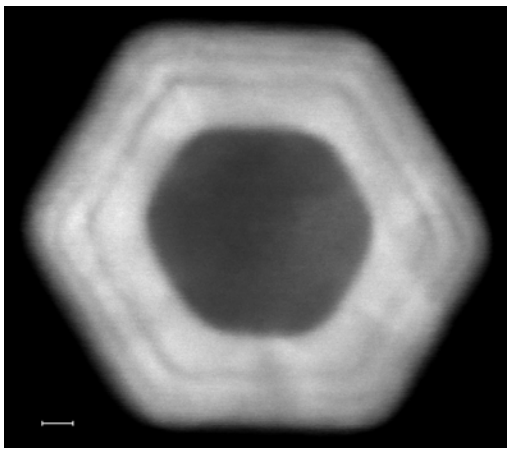

Figure 6: HAADF TEM image of the cross section of a multi-segmented GaP/GaAs wire.

4 ELECTRICAL MEASUREMENTS

The electrical properties of the nanowire/silicon heterointerface were characterized in a two terminal device configuration. For this purpose, the p-doped InP wires grown on a higly p-doped Si (111) substrate with a density of approximately 80 wires per 10x10 μm^2 were embedded in a PMMA layer on which a top metal contact was evaporated. In Figure 7 we show the I-V curve on a semi-logarithmic scale corresponding to the 50x50 μm^2 top contact size measured at room temperature. We note that the currents scale linearly with the area of the top contact.

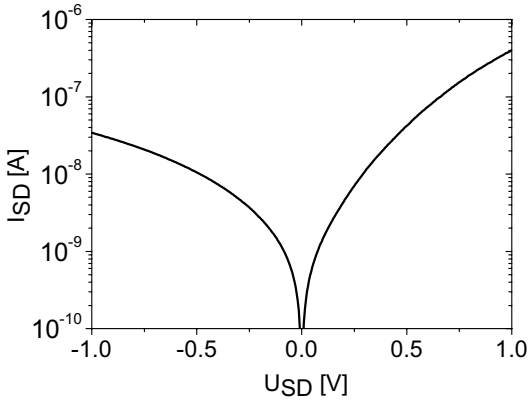

Figure 7: I-V characteristic of p-InP nanowires grown on a p-Si (111) substrate measured at room temperature.

The measured I-V characteristic shows a rectifying behavior with ten times higher current when a positive bias is applied at the top of the wire. The n-InP wires on n-Si substrate (not shown) exhibit higher currents (factor 10^5)

without rectification. This radically different behavior in n- and p-doped samples could be due to the band alignment at the InP/Si interface. This system has not been extensively studied but values in literature report a higher valence band offset (ΔE_v~ 0.46-0.56 eV) than the conduction band offset [11]. It should be noted that the band offset is strongly dependent on the strain distribution across the interface and a significant spread is found in the literature dependent on the growth technique, defect density and crystallographic orientation. Therefore, we can only qualitatively attribute the observed differences to the conduction and valence band offsets. In order to quantitatively characterize the electronic transport across the III-V/silicon interface, the crystallographic quality should be further improved and the doping levels in the wire more accurately controlled.

5 CONCLUSIONS

We have presented a study on the possibility of integration of III-V semiconductor nanowires with silicon. Epitaxial growth of InP, GaP, InAs and GaAs on a silicon (111) substrate was shown III-V and the quality of the heterointerface was investigated. Heterojunctions along the growth direction and in the radial direction have been demonstrated for the GaAs/GaP system with a good control of the interface sharpness. Furthermore, we have presented the first results of electrical characterization of the III-V/Si interface. Further investigation will be needed in order to better understand the band alignement.

REFERENCES

[1] Choi, H.-S.P., IBM Res. & Dev., 46, 133, 2002.

[2] Fang, S.F.; Adomi, K.; Lyer, S.; Morkoc, Zabel, H.; Choi, C.; Otsuka, J. Appl. Phys., 68, R31, 1990.

[3] Cohen, D.; Carter, C.B. J. Microscopy, 208, 84, 2002.

[4] Mårtensson, T.; Svensson, C. P. T.; Wacaser, B. A.; Larsson, M. W.; Seifert, W; Deppert, K.; Gustafsson, A.; Wallenberg, L. R.; Samuelson, L Nano Lett., 4, 1987, 2004.

[5] Bakkers, E. P. A. M.; Van Dam, J. A.; De Franceschi, S.; Kouwenhoven, L. P.; Kaiser, M.; Verheijen, M.; Wondergem, H.; Van der Sluis, P. Nature Materials, 3, 769, 2004.

[6] Wagner, R. S.; Ellis, W. C. Appl. Phys. Lett., 4, 89, 1964.

[7] Hiraki, A.; Lugujjo, E.; Mayer, J. W. J. Appl. Phys., 43, 3643, 1972.

[8] Bakkers, E. P. A. M.; Verheijen, M. J. Am. Chem. Soc., 125, 3440, 2003.

[9] Krishnamachari U.; Borgstrom M.; Ohlsson B. J.; Panev N.; Samuelson L.; Seifert W. Appl. Phys. Lett., 85, 2078, 2004.

[10] M. A. Verheijen, G. Immink, T. de Smet, M. T. Borgström and E. P. A. M. Bakkers, J. Am. Chem. Soc., 128, 1353, 2006.

[11] Mahowald, P.H.; List, R.S.; Woicik, J.; Pianetta, P.; Spicer, W.E. Phys. Rev. B, 34, 7069, 1986.