Novel Nonvolatile Logic Circuits with Three-Dimensionally Stacked Nanoscale Memory Device

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ABSTRACT

Various emerging memories are expected to be applied for alternative nonvolatile memory. However, their potential is not limited to ultra-high-density memory. We propose a nonvolatile 3D logic block using nanoscale emerging memories combined with a conventional logic circuit and discuss some requirements for properties of the emerging memories.

Keywords: emerging memory, 3D stacking, nonvolatile logic circuit

1. INTRODUCTION

The first application of nanodevices using post-Si material for future LSI is expected to be in a new nonvolatile memory (emerging memory) rather than in transistors. Various emerging memories have been proposed for next-generation ultra-high-density memory beyond the limit of the conventional nonvolatile memories, such as magnetic RAM[1], phase change memory [2], solid electrolyte memory (Cu_2S [3], Ag-Ge-Se [4]), organic memory [5] and resistive memory (RRAM [6], SrTiO3 [7]).

However, the potential of the emerging memories is not limited to ultra-high-density memory. By stacking emerging memories on CMOS, additional circuits can be embedded in multiple interconnects, thereby enabling various new functions. For example, hyper-parallel data transfer between memory and logic circuits (ultra-high bandwidth) and reconfigurable logic are achieved with direct 3D-connecting between logic and emerging memories, as shown in Fig.1.

Recently, one of the most valuable functions is the enabling of low power operation of logic circuits since power consumption due to drastically increasing gate leakage current of CMOS will be increasing with miniaturizing of LSI [9]. The most effective method of lowering power is to shut down voltage supply to the logic circuits that are just on standby. This would be feasible in principle, if logic circuits could be "nonvolatile". Although nonvolatile logic circuits could be realized even by combining with conventional 2D semiconductor memories, then circuit area would be increased drastically. We propose a new architecture of 3D circuit using nanoscale memory devices. This architecture realizes more compact circuits with lower power compared to conventional logic circuits by three-dimensionally stacking nonvolatile emerging memories.

Emerging memories are considered to have variable resistances since they have two bistable states with high and low resistance. As for some memories, the resistance is changed by alternately applying long and short voltage pulses. The resistance of other types of emerging memories is reversibly changed by applying forward and reverse voltages alternately. Since such symmetrical write/erase operation is preferable to the direct combination of memory with CMOS logic circuit, the architecture based on the latter type is rather simple.

In the work presented in this paper, we have tried to build a new architecture for a nonvolatile flip flop using 3D memory devices. This is because the role of flip flop in the LSI processor is significant since the processor uses a large number of flip flops for registers and counters. The nonvolatile flip flop could be effective for lowering power in processor. We describe the possibility of the nonvolatile D-type flip flop (D-FF), which is a typical synchronous sequential circuit.

2. 3-DIMENSIONAL NONVOLATILE D-TYPE FLIP FLOP

A typical digital signal processor (DSP) is composed of multiplier, accumulator, RAM, ROM, counters and registers [10]. A large number of counters and registers are used in the DSP, as shown in Fig.2. Both counter and register are composed of synchronous D-FF. The D-FFs are most frequently used as counters or registers in logic circuits. The concept of the nonvolatile D-FF using stacked emerging memories is shown in Fig.3. Since data can be stored in nonvolatile emerging memory, the power supply to both D-FFs and combinational logic circuits connected to them can be shut down. Hence, if non-volatility could be added to the conventional volatile D-FF, it would be possible to reduce the total power

consumption of logic circuits. We have investigated the possibility of making the D-FF nonvolatile so as to reduce power consumption.

2.1. CMOS Master-Slave D-FF

The circuit diagram of the CMOS master-slave nonvolatile D-FF is depicted in Fig.4. Each nonvolatile D-FF consists of an emerging memory (R1) and reference resistance (R0) connected in series with cross-coupled inverters in the slave side. R1 is written when clock signal is low, and the resistance of R1 has high (OFF) or low (ON) state depending on input data D [8]. Since the source contacts for MOSFETs in the downside inverter are connected with clock signals (CK, $\overline{CK}$), the downside inverter works as an inverter when clock signal is low, and as a transmitter when clock signal is high. If the supply voltage is turned back after powering off as recall operation, the cross-coupled inverter on the slave side will be metastable. In that case, the final Data Q value is determined by the delay which, in turn, depends on the resistance of R1 and R0. If the resistance of R1 is greater than that of R0, then the final Data Q value will go to logic "1" because the time delay through R1 is longer than that through R0. The time delay through the higher resistance is longer than the time delay through the lower resistance. Using this phenomenon, we demonstrate the recall operation of nonvolatile D-FF by simulation, and discuss whether the margin for recall operation can be performed.

Figure 5 shows a simulation result for the recall operation in CMOS master-slave D-FF. We use SPICE based on the BSIM3v3 model. The reference resistance R0 is fixed to be 1kΩ. Since the node voltage of the low resistance side (R0 side: V3, V4) is high, data can be read correctly (="pass") as shown in Fig. 5 (a). On the other hand, even if data can be read correctly, read-out time is over 10ns in some cases, as shown in Fig. 5 (b).

The results of the simulation are summarized in Fig.6, indicating the combinations of resistance and capacitance pass in the simulation. The suitable resistance ratio (=R1 (OFF) / R0) for fast and stable recall operation is between several and 10^3. The higher resistance of an emerging memory (R1 (OFF)) must not be too large, since too much time will then be taken for decision on read-out data when R1 (OFF) is more than 5MΩ. It is also required that load capacity should be more than 1 femtofarad.

Because the OFF-resistance of an SEM is too large, it is considered unsuitable for use in this circuit. The endurance for write/erase operation is required to be over 10^{14} [8]. From this viewpoint, the most feasible device is spin-injection MRAM [11]. Though the resistance change is very low at the present, increase of over 200% can be expected by using half-metal magnetic layers or single-crystal tunneling layers.

2.2. Master-slave and Edge-Triggered D-FF consisting of NAND-based RS latch

Fig.7 (a) shows the nonvolatile RS latch. The nonvolatile RS latch can be utilized as RS latch in the master-slave D-FF shown in Fig.7 (b) or RS latch in edge-triggered D-FF shown in Fig.7(c). Since both D-FF circuits include nonvolatile RS latches, the output data are stored even when power is not supplied.

The nonvolatile RS latch includes two emerging memories, which are serially combined with cross-coupled NAND gates. A write operation occurs when S and R are in opposite states (e.g., S=0 and R=1 or R=1 and S=0). The output signal Q written into the emerging memories follows the reset signal R. When the power is turned back on to nonvolatile RS latch, a recall operation is performed by applying logic "1" to both the set (S) and reset (R) inputs to nonvolatile RS latch. Under that condition, NAND gates can be represented as inverters. Therefore the behavior of nonvolatile RS latch is similar to that of cross-coupled inverters as shown in Fig.5. If the resistance of R2 is greater than that of R3, then the final Data Q value will go to logic "1" and the output value $\overline{Q}$ will go to logic "0" because the time delay through R2 is longer than that through R3. Conversely, if the resistance of memory R3 is larger than that of R2, the output Q will go to logic "0" and the $\overline{Q}$ will go to logic "1". Therefore, the previous data that was stored in nonvolatile RS latch before the power was turned off is recalled and reinstated in nonvolatile RS latch.

In the nonvolatile master-slave D-FF shown in Fig.7 (b), data D is input to the D Latch when the clock signal G becomes high and is latched into D latch on the high to low transition of clock signal G. The output signals Q and $\overline{Q}$ from D latch are input to NAND gates, respectively, along with the clock signal. The output signals from these NAND gates are then input to the set (S) and reset (R) inputs, respectively, of nonvolatile RS latch. The output signal Q is the data stored in the nonvolatile RS latch. When the clock signal G is low, the input signals S and R to nonvolatile RS latch are the inverted symbols Q and $\overline{Q}$ from D latch. However, if the clock signal G is high, logic high is input to both S and R of RS latch.

In the nonvolatile edge-triggered D-FF shown in Figure 7(c), data D is input to the S terminal of conventional RS latch 1 and the clock signal is input to the R terminal of conventional RS latch 1. The Q output signal from conventional RS latch 2 is input to the S terminal of conventional RS latch 1 while the output signal $\overline{Q}$ from conventional RS latch 1 is input to an AND gate along with the clock signal. The output signal $\overline{Q}$ from conventional RS latch 1 is input to the S terminal of nonvolatile RS latch while the signal from conventional RS latch 2 is input to the R terminal of nonvolatile RS latch. As a result, data D is stored in the flip-flop formed by conventional RS latch 1, 2 and in nonvolatile RS latch on a rising edge of the clock signal.

Fig.8 shows the results of simulation for the D-FF and recall operations in the nonvolatile master-slave D-FF, as shown in Fig. 7(b). We also use SPICE based on the BSIM3v3 model. These waveforms indicate the transitions of voltage in D-FF for D-FF operation and recall operation. The opposite voltage is applied to emerging memories (R2 and R3) when clock signal G is in low state. Then the resistances of R2 and R3 change

into high or low depending on the output signal Q, for example, R2=high resistance and R3=low resistance in the case of Q="1". In recall operation, the previous data that were stored in R2 and R3 can be read correctly when clock signal G is in high state.

3. CONCLUSION

The nonvolatile D-FF is realized by combining the CMOS logic gate with the emerging memory 3-dimensionally stacked on the CMOS. We propose three kinds of nonvolatile D-FF with 3D emerging memories. We suggest that the most feasible emerging memory for the nonvolatile D-FF is spin injection MRAM from the viewpoint of endurance. The nonvolatile D-FF is a functional component for lowering power in logic LSI.

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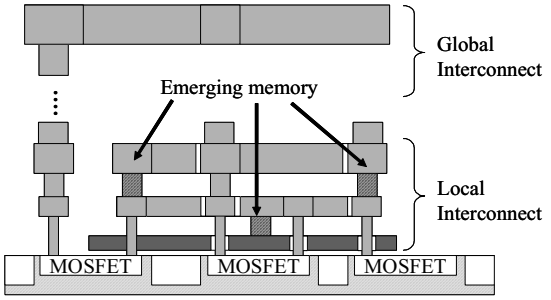

Fig.1 Cross sectional schematic of 3-dimensionally stacked memories in local interconnect

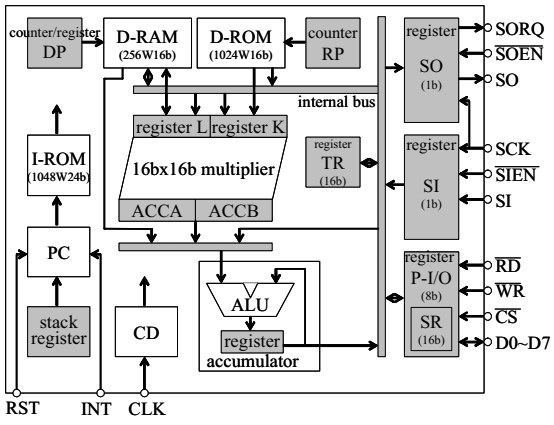

Fig. 2 Architecture of typical digital signal processor

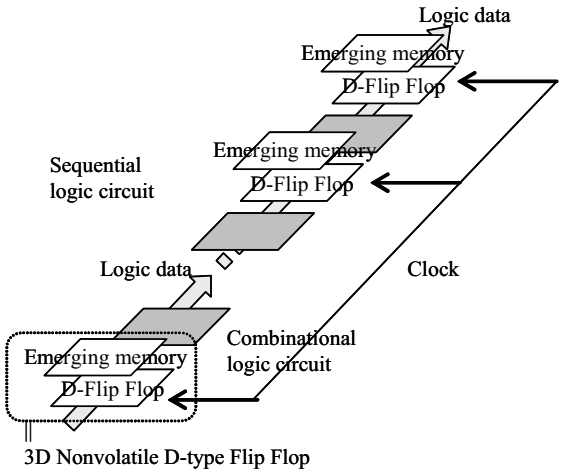

Fig.3 Concept of the logic circuit with nonvolatile D-FF