

2D Quantum Mechanical Device Modeling and Simulation: Single and Multi-fin FinFET

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ABSTRACT

We propose a novel device structure ($\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ hetero-structure), which is called “center-channel (CC) double-gate (DG) MOSFET.” The device performance of the proposed FET structure was investigated with our two-dimensional quantum-mechanical simulator which is based upon the self-consistent solution of Poisson-Schrödinger equations and the current continuity equation. The CC operation of CC-NMOS is confirmed by considering the band lineups as well as the lowest energy wave function. Especially, the lowest energy wave function of CC-MOSFET is carefully compared with those of the conventional DG-NMOS in order to observe the distinct feature of the proposed FET structure. Furthermore, device optimization for the CC operation and short-channel effects (SCE) was performed in terms of Ge concentration, gate length (L_g), and $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ scale variation.

Keywords: Center-Channel operation, double gate MOSFET, quantum mechanical modeling and simulation, coupled Poisson and Schrödinger equations, Short-channel effects

1 INTRODUCTION

Recently, approaches for nano-scale semiconductor devices place a lot of emphasis on materials and structures [1-2]. The enhancement of carrier mobility in the conduction channel needs high-mobility materials such as $\text{Si}_{1-x}\text{Ge}_x$ and strained-Si. However, conventional MOSFET with strained-Si channel has some disadvantages such as the limit of scaling, high-electric field in the channel, and corresponding degradation of mobility. For the solution of these problems, we propose and simulate a high-performance center-channel (CC) double-gate (DG) structure incorporating with the materials of $\text{Si}_{1-x}\text{Ge}_x$ and strained-Si. To fulfill the numerical simulation of nano-scale structures such as DG MOSFET, we need to obtain a self-consistent solution of the coupled Poisson-Schrödinger equations. The CC-NMOS device exhibits the enhancement of current drive and switching speed caused by decrease of

surface roughness scattering and mobility enhancement of strained-Si channel.

2 NUMERICAL MODEL FOR COMPUTER SIMULATION

The two-dimensional (2-D) QM model is based on the self-consistent solution of coupled Poisson-Schrödinger equations to describe the effect of strain on the band structure of Si and bound states. The 2-D QM model is based on the self-consistent solution of Poisson-Schrödinger equations in a simultaneous manner [3].

$$\nabla \cdot [\varepsilon(x, y) \nabla \Phi(x, y)] = -\rho(x, y), \quad (1)$$

$$\rho(x, y) = q[-n(x, y) + p(x, y) + N_D^+(x, y) - N_A^-(x, y)], \quad (2)$$

$$-\frac{\hbar^2}{2} \nabla \cdot \left[\frac{1}{m^*} \nabla \Psi_n(x, y) \right] + V(x, y) \Psi_n(x, y) = E_n \Psi_n(x, y), \quad (3)$$

where ε is the dielectric constant, Φ the electrostatic potential, ρ the total charge density, n and p the electron and hole concentrations, N_D^+ and N_A^- the ionized donor and acceptor concentrations, $\Psi_n(x, y)$ the wave function of n^{th} eigenstates, \hbar the Planck's constant divided by 2π , $m^*(x, y)$ the effective mass, E_n the energy of the n^{th} eigenstates, and V the potential energy which is given by $V = \Delta E_c(x, y) - q\Phi(x, y)$. Here, $\Delta E_c(x, y)$ is the band offset in the conduction band.

For the solution of Schrödinger equation, we used mixed Dirichlet and von-Neumann boundary conditions. Here, the Schrödinger equation is solved with both Dirichlet and von-Neumann boundary conditions, then the density for each state is averaged between the two solutions to minimize numerical boundary effects. By solving the Schrödinger equation, we obtain the quantized states which are occupied with the local quasi-Fermi levels. The two-dimensional quantum electron density is found by using

$$n(x, y) = \frac{2}{\pi\hbar} \sqrt{2m^*k_B T} \sum_j |\Psi_j(x, y)|^2 \times F_{-1/2} \left(\frac{E_F - E_j}{k_B T} \right), \quad (4)$$

where E_j and $\Psi_j(x, y)$ are the energy and the wave function of the j^{th} eigenstate, $E_F(x, y)$ the Fermi level, and F_k the Fermi-Dirac integrals of order k . These integrals are defined as follows:

$$F_k(\eta) = \frac{1}{\Gamma(k+1)} \int_0^\infty \frac{u^k du}{1 + e^{u-\eta}}, \quad k \geq -1 \quad (5)$$

and also have the following property

$$\frac{d}{d\eta} F_k(\eta) = F_{k-1}(\eta), \quad k \leq -1 \quad (6)$$

We obtain the semi-classical current solution from the 1st moment of Boltzmann equation by adopting a simple drift-diffusion model for the electron current:

$$J_n(x, y) = \mu_n(x, y) n(x, y) \nabla E_{Fn}(x, y), \quad (7)$$

The continuity equation for current density is given by

$$\nabla \cdot J_n(x, y) = -R(x, y), \quad (8)$$

In order to obtain self-consistent QM solutions, we have employed an iterative procedure [4]. We start out by calculating the electric potential. Next, the program calculates a charge distribution using an iteration scheme. Thereafter, the program determines self-consistent solutions of Poisson-Schrödinger and current equations [4]. The Newton method has been employed with a constraint that should satisfy error criteria as outlined in [3].

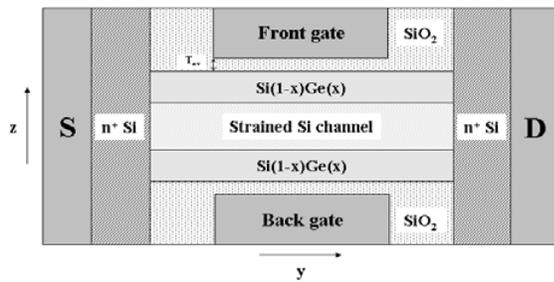


Figure 1: Schematic diagram of CC-NMOS considered in this work.

Figure 1 schematically shows the CC-NMOS considered in this work. Two metal gates with gate length L_g and work function $\Phi_M = 4.1$ eV are located symmetrically on both sides of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ heterostructure. The source and drain regions are modeled as ohmic contacts with a doping of $2 \times 10^{20}/\text{cm}^3$, and the

channel region under the gate is undoped. The oxide thickness (T_{ox}) is 2 nm, and L_g varies from 10 nm to 80 nm.

3 SIMULATION RESULTS

In this work, we confirmed the CC operation, the enhancement of drive current and G_m , and short-channel effects (SCE) of the proposed CC-NMOS structure.

First, we confirmed the CC operation of CC-NMOS through the band lineups, lowest energy wavefunction, and electron density. Figure 2 shows the band lineups of CC-NMOS under the condition of $L_g=30$ nm, $V_d=0.1$ V by varying V_g from -1.5V to 1.5 V. From this, we understand the band offsets, the formation of quantum-well from $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ heterostructure of CC-NMOS, and corresponding CC operation [1]. The lowest energy wavefunction of CC-NMOS is compared with that of DG-NMOS through Fig. 3 and Fig. 4 at the condition of $L_g=30$ nm, $V_d=0.1$ V, and $V_g=1.5$ V. Contrary to DG-NMOS, the wavefunction of CC-NMOS is confined to the center of channel meaning the CC operation.

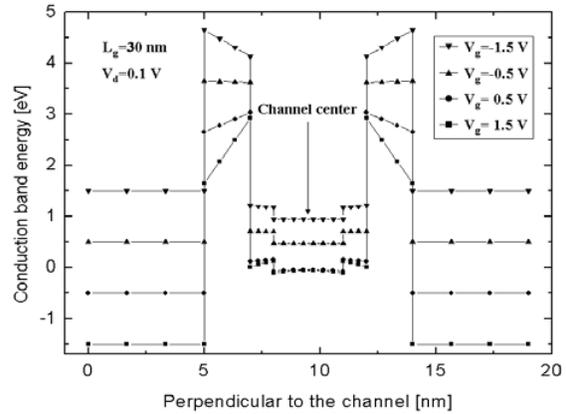
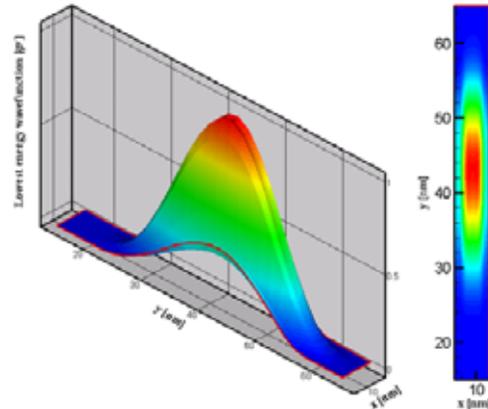


Figure 2: Band lineups of CC-NMOS for $L_g=30$ nm, $V_d=0.1$ V, and V_g from -1.5 to 1.5 V.



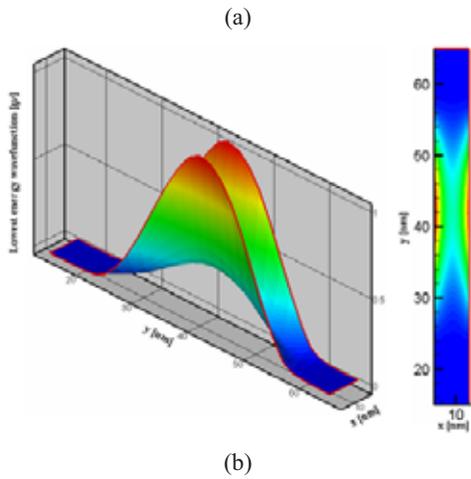


Figure 3: Lowest energy wavefunction for $L_g=30$ nm, $V_d=0.1$ V, and $V_g=1.0$ V. (a) CC-NMOS, (b) DG-NMOS.

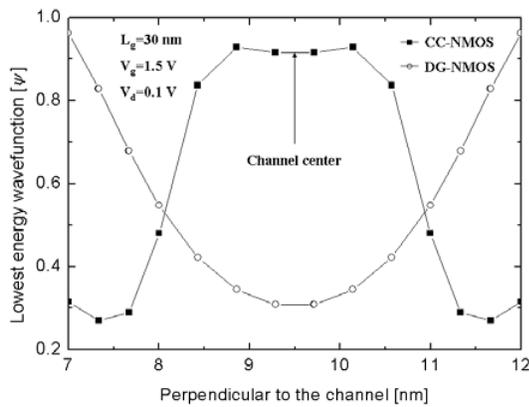


Figure 4: Comparison of lowest energy wavefunction of CC and DG-NMOS for $L_g=30$ nm, $V_d=0.1$ V.

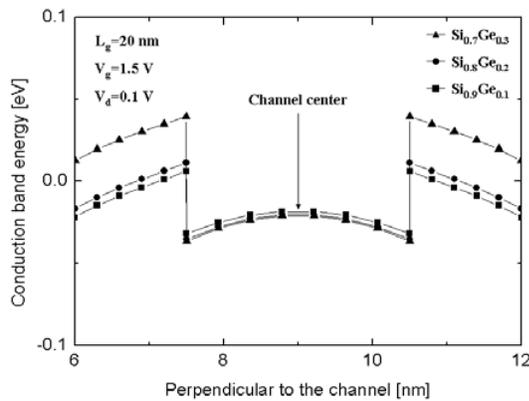


Figure 5: Conduction band energy of CC-NMOS for $L_g=20$ nm, $V_d=0.1$ V, and $V_g=1.5$ V with various Ge concentration.

Figure 5 shows the conduction band energy of CC-NMOS for $L_g=20$ nm, $V_d=0.1$ V, and $V_g=1.5$ V with various Ge concentration. This result demonstrates that larger Ge concentration is good for the CC operation due to the band offsets of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ hetero-structure.

Finally, we estimated the SCE of CC-NMOS by performing the simulation with respect to L_g and $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ scale. Figure 6 and 7 show the I_d - V_g curves and transconductance (G_m) for CC-NMOS performed under the condition of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ varying from 2 to 32 nm. And the conduction band energy of CC-NMOS for $V_d=0.1$ V, $V_g=1.5$ V, and L_g from 10 to 80 nm is showed in Fig. 8. We performed the structural optimization of SCE in terms of subthreshold swing, threshold voltage (V_t) roll-off, drain-induced barrier lowering (DIBL) through Figs. 9, 10, and 11. From these results, we confirmed that CC -NMOS show excellent subthreshold behaviors and successfully suppress the SCE.

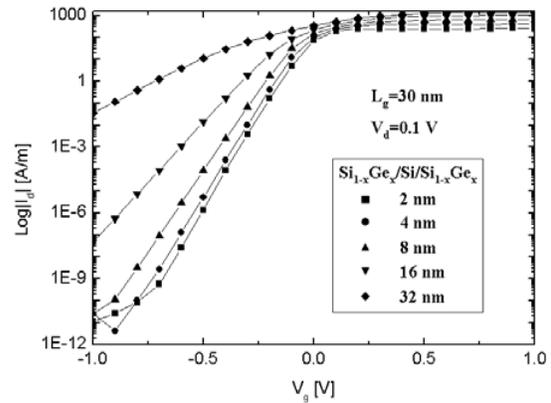


Figure 6: I_d - V_g characteristics for CC-NMOS with $\text{Si}_{1-x}\text{Ge}_x/\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ of 2~32 nm, $V_d=0.1$ V, and $L_g=30$ nm.

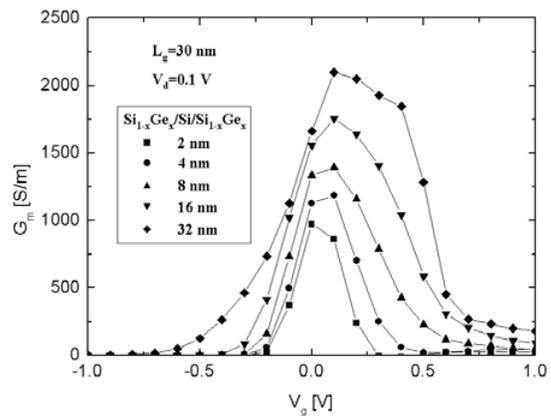


Figure 7: G_m characteristics of CC-NMOS under the same condition of Fig. 6.

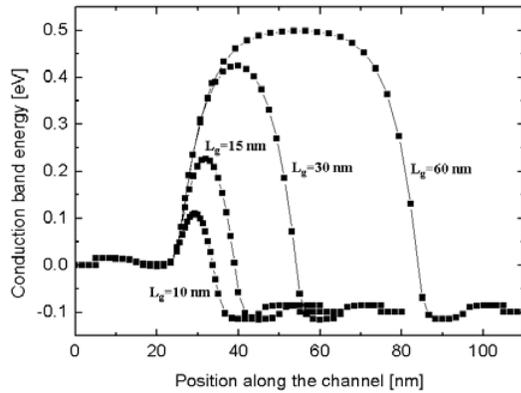


Figure 8: Conduction band energy of CC-NMOS for $V_d=0.1$ V, $V_g=1.5$ V, and L_g from 10 nm to 80 nm.

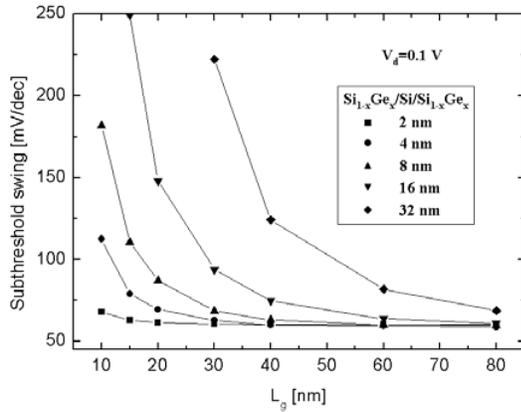


Figure 9: Subthreshold swing of CC-NMOS in terms of L_g at $V_d=0.1$ V at various $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ scales.

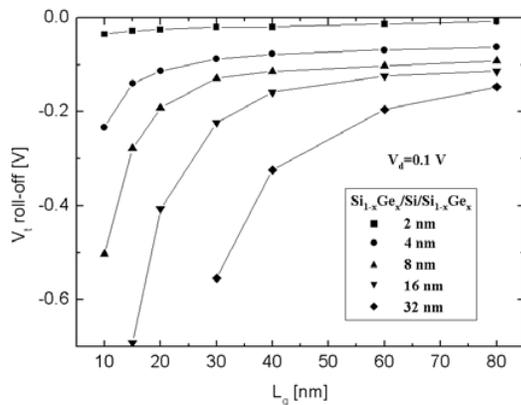


Figure 10: V_t roll-off of CC-NMOS in terms of L_g at various $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ scales.

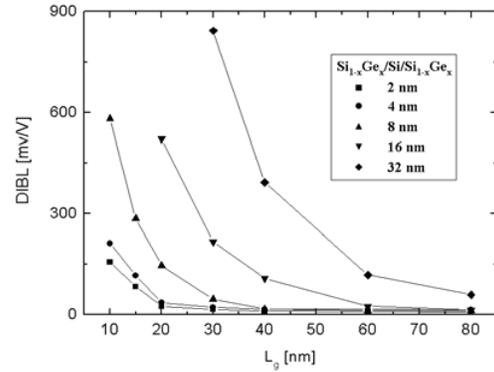


Figure 11: DIBL of CC-NMOS in terms of L_g at various $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ scales.

4 CONCLUSION

In this paper, we report our two-dimensional numerical modeling and simulation results for center-channel (CC) double-gate (DG) MOSFET with comparison to those of conventional DG structure. CC operation of CC-NMOS is confirmed by band lineups and lowest energy wavefunction. The simulation results also reveal that the short-channel effects are appreciably suppressed. Our simulation results imply that CC-NMOS structure is a promising candidate for implementing the sub-20nm MOSFETs.

5 ACKNOWLEDGEMENT

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