Room-Temperature InAlAs/InGaAs Planar Tunneling-coupled Transistor

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1. Introduction

In recent years, numerous circuits have been demonstrated based on tunneling devices, ranging from memory/digital logic to mixed-signal circuits such as analog-to-digital converters (ADC) [1]. Also, there is growing interest in quantum MMICs. [2] Compared to circuits fabricated with conventional HEMTs or HBTs, these tunneling-based circuits offer circuit performance with reduced power dissipation and circuit complexity at a given speed. However, due to the lack of high performance and integrable tunneling transistors, most of the circuits have been demonstrated either in the form of resonant tunneling diode (RTD) or RTD/FET or RTD/HBT. [3-4] Various tunneling transistors have been proposed and demonstrated mostly in vertical forms.[5] Although these versions offer input-output isolation, both gain and control of negative-differential-resistance (NDR) have been limited. On the other hand, tunneling transistors in planar form, being straightforward to integrate, have been demonstrated, but at low temperatures. [6]

In this paper, we report the first experimental demonstration of InAlAs/InGaAs *planar tunneling-coupled transistors at room temperature*, in which tunneling characteristics such as negative differential resistance (NDR) and peak current are controlled with high gain and transconductance by a surface Schottky gate similar to state-of-the-art HEMTs. Functionality of the device can be switched between HEMT mode and tunneling transistor mode. The fabrication process is fully compatible with conventional HEMT processes, offering a fully integrable and scalable tunneling transistor technology. The planar tunneling-coupled transistors were fabricated with closely-coupled dual-channel HEMT heterostructures based on InGaAs/InAlAs/InP or InGaAs/InAlAs/AlAs/InP structures by providing independent electrical contacts to each HEMT channel. The current-voltage characteristics are determined by an interwell and intersubband tunneling.

2. Result

The fabrication process was done using an I-line Cannon stepper on full 3-inch wafers with implanted back-gates defined prior to MBE growth of closely-coupled dual-channel HEMT layers. The highest mobility of the closely-coupled dual-channel HEMT layers observed so far is 9600 cm^2/Vs at room temperature.

Figure 1 shows measured current-voltage characteristics of an InAlAs/InGaAs tunneling-coupled transistor with top-gate voltage stepped in -0.1 V increments. While the top-gate controls the tunneling peak current, the tunneling peak voltage is also shifted as a function of the top-gate voltage, as expected in interwell and intersubband tunneling between two separate two-dimensional electron gas (2DEG) layers. The tunneling characteristics are also modulated by back-gate voltage.

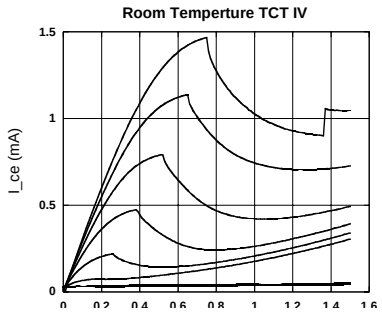

Figure 1. Measured room-temperature tunneling I-V characteristics as a function of top-gate voltages of InAlAs/InGaAs planar tunneling-coupled transistors

We have fabricated tunneling-coupled transistors with AlAs/AlGaAs/AlAs or AlGaAs/AlAs/AlGaAs tunneling barriers, in which total barrier thickness is 75 A. Room-temperature peak-to-valley current ratio (PVR) is 5:1. The peak current density is 2.4 x 10^3 A/cm^2 per gate area. The peak current density can be increased with a thinner tunneling barrier. Figure 2 shows the measured tunneling transfer curve. As top-gate voltage increases from -1 V, TCT current also increases initially, leading to a

current also increases initially, leading to a positive transconductance (gm). Near Vgs = -65 mV, TCT current was switched to low, indicating an excellent gate-induced switching of the tunneling current. The tunneling-coupled transistors can also be operated in HEMT-mode, as shown in Figure 3, allowing fully integrable circuit concepts.

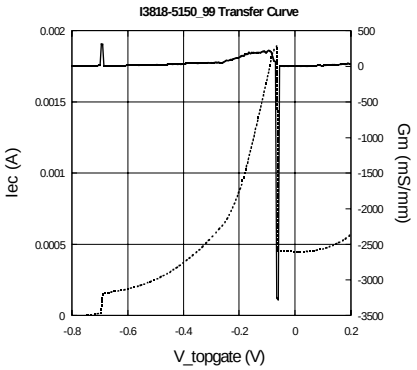

Figure 2. Room-temperature tunneling transfer curve of the planar tunneling-coupled transistor showing gate voltage

3. Summary

In summary, for the first time, room-temperature planar tunneling-coupled transistors, fully compatible with HEMT process, have been demonstrated with excellent gate control of NDR and gate-induced switching. This work was sponsored by the Director's Innovation Initiative of the National Reconnaissance Office.

4. Reference

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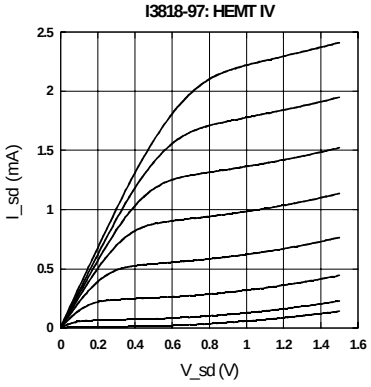

Figure 3. Measured room-temperature HEMT I-V characteristics when the tunneling-coupled transistor is operating in HEMT mode

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