Compact Modelling of High-Voltage LDMOS Devices

A.C.T. Aarts, R. van der Hout, R. van Langevelde, A.J. Scholten,
M.B. Willemsen, and D.B.M. Klaassen

Philips Research Laboratories
Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands, annemarie.aarts@philips.com

ABSTRACT

In this paper various modelling approaches for Laterally Double-Diffused MOS (LDMOS) devices are discussed. Characterisation results for the new compact LDMOS model called MOS Model 20 are presented. Measurements of the dc-current, its conductances and the capacitances obtained from Y-parameters of an LDMOS device, show that MOS Model 20 provides accurate descriptions in all regimes of operation. For future developments, the inclusion of quasi-saturation in MOS Model 20 is demonstrated. Finally, the consequence of the lateral non-uniformity of the LDMOS device for compact modelling is discussed.

Keywords: LDMOS, compact modelling, high-voltage MOS, MOS Model 20, quasi-saturation.

1 INTRODUCTION

1.1 LDMOS Devices

High-voltage LDMOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies and RF-power amplifiers. In Figure 1 a cross-section of an LDMOS device is given. The p-well (B) is diffused from the source-side under the gate (G), thus forming a graded inversion channel region. To withstand the high voltages applied between source (S) and drain (D), a lightly doped n^--drift region is made. In this specific case, the gate extends over the drift region, so that in the linear operating regime an accumulation layer forms under the thin gate oxide in the drift region. The internal drain (Di) represents the point where the channel region turns into the drift region.

Optimal design of these power circuits requires LDMOS models for circuit simulation, which accurately describe the electrical characteristics over a wide range of biases. To take the specific high-voltage aspects of an LDMOS device into account, dedicated LDMOS models are necessary.

1.2 Modelling Approaches

1.2.1 Sub-Circuit Models

A frequently followed approach in high-voltage modelling is to describe the LDMOS transistor by a sub-

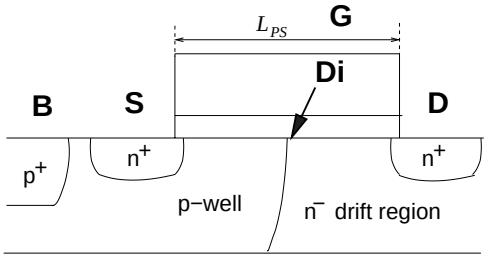

Figure 1: Cross-section of a n-type LDMOS transistor, with the gate (G) extending over the lightly doped n^--drift region. The p-well is diffused from the source-side, thus forming a graded channel region.

circuit model (also called macro model) [1]-[5]. In this approach, a circuit model for the channel region is put in series with a circuit model for the drift region. As a result, the sub-circuit model contains an additional circuit node, and the circuit simulator solves, numerically, the potential at this node. The advantage of the sub-circuit model approach is its flexibility, which is especially valuable if one needs to build models for various high-voltage transistors with different device structures. Furthermore, the charge partitioning for the channel region is described independently from that of the drift region, and during circuit simulation the currents through the device are obtained automatically with the solution of the potential at the circuit nodes. The disadvantage of sub-circuit models, however, is that there is no control during circuit simulation on the behavior of the potential at the additional circuit nodes. Consequently, sub-circuit models may give rise to an increase of computation time, or, even worse, may have difficulty to reach convergence at all. Furthermore, most models [1]-[5] lack an accurate description of one or more specific device characteristics.

1.2.2 Single (Compact) Models

Another approach in LDMOS modelling is to define a single model, mostly called compact model, in which the potential at the internal drain is solved inside the model itself [6]-[12]. This approach remedies the disadvantages of the sub-circuit model approach mentioned above. For the determination of the internal drain potential two

methods are possible, that is, a numerical iteration procedure (cf. [6]-[9]) and an analytical solution (cf. [10]-[12]). As long as care is taken that the iteration procedure is always converging to the desired solution and the convergence error is sufficiently small, the numerical iteration approach is valuable and gives sufficiently smooth characteristics. The drawback of the models in [6]-[9], however, is that the sub-threshold regime is not included. In the analytical solution method, the internal drain potential is *explicitly* expressed in terms of the external terminal voltages. Unfortunately, the models in [10] and [11] lack a sufficiently accurate description, and the model in [12] has been found to be limited due to the occurrence of non-convergence during circuit simulation. In contrast to a sub-circuit model, in a single model it is necessary to have a nodal charge model for the whole device, which combines the charges of the channel region to those of the drift region. The capacitances for the description of the small-signal currents are, on their turn, derived from this nodal charge model.

2 MOS MODEL 20

To avoid convergence problems in sub-circuit modelling, we have developed a new, single (compact) model for LDMOS devices, called MOS Model 20 [13]. The model is based on [12], and it includes all specific high-voltage aspects. The source code and documentation of MOS Model 20 are available in the public domain [14], and a detailed derivation of the model can be found in [15]. The model is surface-potential-based, and it incorporates mobility reduction due to the vertical electrical field, velocity saturation in the channel region, drain-induced barrier lowering and static feedback. MOS Model 20 is aimed for long-drift-region devices, since it is assumed that velocity saturation occurs in the channel region. In this section, we provide additional characterisation results using MOS Model 20.

2.1 DC-Model

In our compact modelling approach, expressions for the channel region current $I_{\rm ch}$ as well as for the drift region current $I_{\rm dr}$ are derived, both in terms of the known external drain-, gate-, source- and bulk voltages $V_{\rm D}$, $V_{\rm G}$, $V_{\rm S}$ and $V_{\rm B}$, respectively, as well as in terms of the internal drain voltage $V_{\rm Di}$. In contrast to a sub-circuit model, this internal drain voltage is expressed explicitly in terms of the external terminal voltages. The expression for this internal drain voltage is derived by equating $I_{\rm ch}$ to $I_{\rm dr}$. Next, the internal drain voltage is used to calculate (also in an explicit way) the surface potentials, in which the final drain-to-source current $I_{\rm DS}$ is formulated. In this way, $I_{\rm DS}$ is surface-potential based and it is explicitly expressed in terms of the external terminal voltages.

In Figures 2 and 3 the dc-results of a 12V SOI-LDMOS transistor are given. The device has a structure like the one in Figure 1, with oxide thickness $t_{\rm ox} = 38$ nm. The threshold voltage of the device is about 2 V. For characterisation different mask widths $W_{\rm mask}$ and gate mask lengths $L_{\rm PS}$ have been used, as well as different ambient temperatures T. In addition, a thermal sub-circuit is used in which the temperature rise due to self-heating is calculated [4]. In the figures, symbols correspond to the measurement data, while the solid lines represent MOS Model 20.

In Figure 2 the drain current and the transconductance are plotted versus gate-source voltage. We observe that the model is accurate over the whole gate-bias range, thanks to the inclusion of the effect of the gate extending over the drift region. In Figure 3 the drain current and the output conductance are plotted versus drain voltage. We observe that for $V_{\rm GS} = 6$, 9 and 12 V, the output conductance becomes negative, due to self-heating. We conclude that the dc-behaviour is very well described by MOS Model 20, over the whole range from the linear operating regime into saturation, for both low- and high gate voltages.

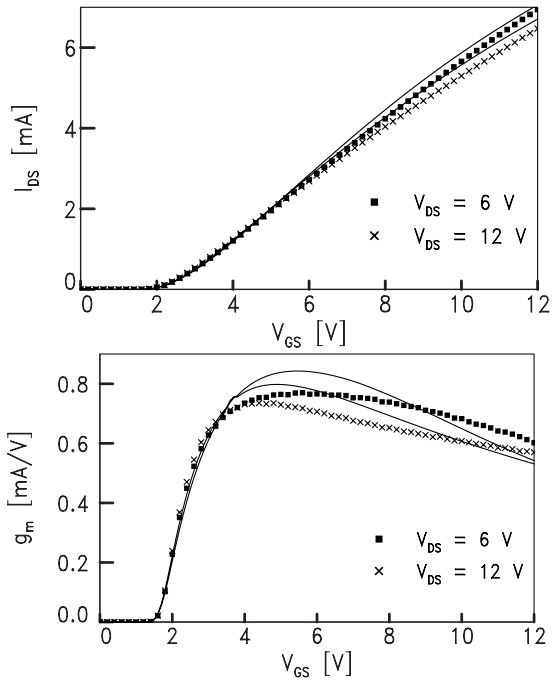

Figure 2: Measured (symbols) and modelled (solid lines) drain current $I_{\rm DS}$ and transconductance $g_{\rm m} = \partial I_{\rm DS}/\partial V_{\rm GS}$ for $V_{\rm DS} = 6$ and 12 V, and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 17$ μm, $L_{\rm PS} = 1.6$ μm and $T = 25$ ^{o}C.

2.2 Nodal Charge Model

For simulation of the time-dependent behaviour, MOS Model 20 has a nodal charge model. From this nodal

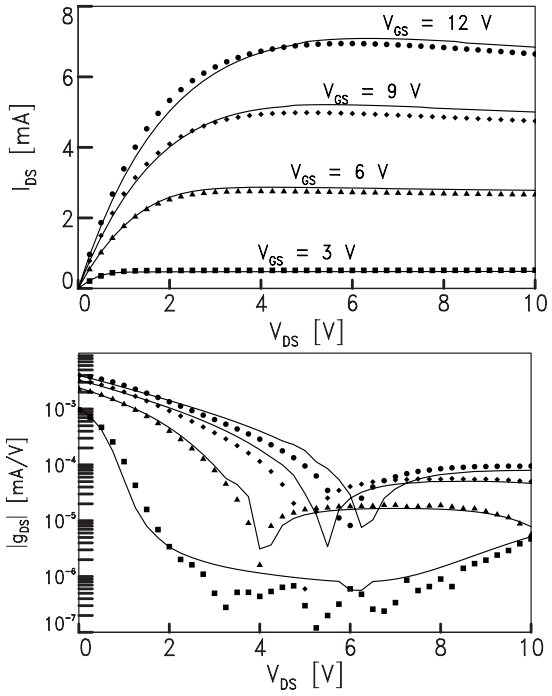

Figure 3: Measured (symbols) and modelled (solid lines) drain current $I_{\rm DS}$ and output conductance $g_{\rm DS} = \partial I_{\rm DS}/\partial V_{\rm DS}$ for $V_{\rm GS} = 3$, 6, 9 and 12 V, and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 17$ μm, $L_{\rm PS} = 1.6$ μm and $T = 25$ ^{o}C.

charge model the capacitances C_{ij} are determined as the derivatives of the nodal charges Q_i to the terminal voltages V_j according to

$$C_{ij} = (2\delta_{ij} - 1)\,\frac{\partial Q_i}{\partial V_j}, \qquad i,j = {\rm D,G,S,B}, \tag{1}$$

where δ_{ij} is the Kronecker delta.

Since the LDMOS device consists of a p-type channel region and an n-type drift region, a lateral non-uniformity exists in the device. As a result, the drift region has, for instance, a lower threshold voltage than the channel region. Consequently, below the threshold voltage of the device the electron charge can only come from the drain-side. To take the lateral non-uniformity into account in the model, a so-called *modified* Ward-Dutton charge partitioning scheme for the distribution of the electron charge underneath the thin gate oxide has been developed [12]. This scheme identifies two limits, the first one corresponds to a distribution according to the conventional Ward-Dutton charge partitioning scheme [16], which is valid for the gate voltage sufficiently large. In the second limit, which is valid for the gate voltage sufficiently small, all electron charge of the drift region is attributed to the nodal drain charge.

The nodal charge model is verified by high-frequency measurements on a 14V SOI-LDMOS transistor with bulk and source tied together. The measurements were performed by use of an S-parameter analyzer at a frequency f of 100 MHz, from which the Y-parameters are determined. The capacitances of the device without gate resistance $R_{\rm G}$ are determined from the Y-parameters including gate resistance, by means of:

$$\begin{aligned} C_{\rm GG} &= \frac{{\rm Im}\{Y_{\rm GG}\}}{\omega}, \qquad C_{\rm GD} = \frac{{\rm Im}\{Y_{\rm GD}\}}{\omega}, \\ C_{\rm DG} &= \frac{{\rm Im}\{Y_{\rm DG}\}}{\omega} - R_{\rm G}{\rm Re}\{Y_{\rm DG}\}\frac{{\rm Im}\{Y_{\rm GG}\}}{\omega}, \\ C_{\rm DD} &= \frac{{\rm Im}\{Y_{\rm DD}\}}{\omega} - R_{\rm G}{\rm Re}\{Y_{\rm DG}\}\frac{{\rm Im}\{Y_{\rm GD}\}}{\omega}, \end{aligned} \tag{2}$$

where $\omega = 2\pi f$. The device has a structure like the one in Figure 1, with oxide thickness $t_{\rm ox} = 60$ nm. The threshold voltage of the device is about 3 V. For characterisation different mask widths $W_{\rm mask}$ and gate mask lengths $L_{\rm PS}$ have been used. To model the capacitance of the pn-junction between the p-well and n$^-$-drift region we used an additional junction model.

In Figure 4 we observe that the capacitance $C_{\rm GD}$ is accurately modelled. For more plots showing the comparison between measurements and model for the gate-related capacitances $C_{\rm GD}$ and $C_{\rm GG}$, we refer to [15]. Notice that in the model, the potential at the internal drain automatically accounts for the correct behaviour of the gate-related capacitances. Thus, the nodal gate charge model adequately describes the small-signal currents through the gate.

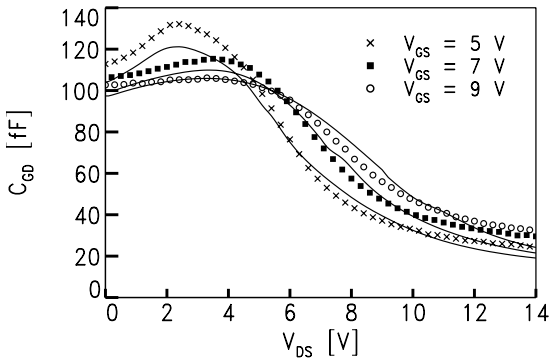

Figure 4: Measured (symbols) and modelled (solid lines) capacitance value $C_{\rm GD}$ versus $V_{\rm DS}$, for $V_{\rm GS} = 5$, 7 and 9 V, for $W_{\rm mask} = 50$ μm and $L_{\rm PS} = 5$ μm.

In Figures 5 and 6 the capacitances $C_{\rm DG}$ and $C_{\rm DD}$ are plotted, both representing the small-signal current through the drain terminal. Notice that these capacitances also depend on the gate resistance and the capacitance values $C_{\rm GG}$ and $C_{\rm GD}$; see (2). For the capacitances $C_{\rm DG}$ and $C_{\rm DD}$ the modified Ward-Dutton charge partitioning scheme applies. In Figures 5 and 6 we observe that for both low- and high gate voltages (which are the two limits identified in the modified

Ward-Dutton charge partitioning scheme) the model adequately describes the capacitive behaviour. However, at the transition around the threshold voltage of the device, we observe that MOS Model 20 somewhat underestimates the capacitance values. The reason is the neglect in MOS Model 20 of the diffused doping profile in the channel region. Thus, the modified Ward-Dutton charge partitioning scheme reasonably predicts the capacitances at its two limits, but a more physics-based description at the transition is desired, and the diffused doping profile needs to be taken into account.

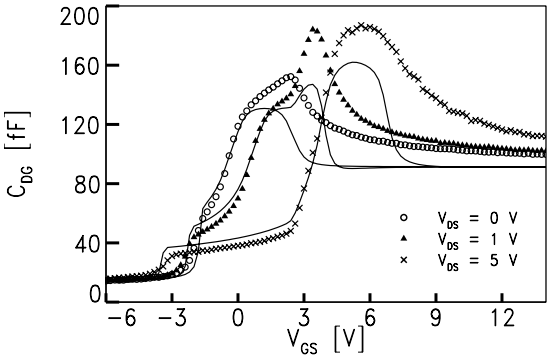

Figure 5: Measured (symbols) and modelled (solid lines) capacitance value $C_{\rm DG}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 0$, 1 and 5 V, for $W_{\rm mask} = 50$ μm and $L_{\rm PS} = 5$ μm.

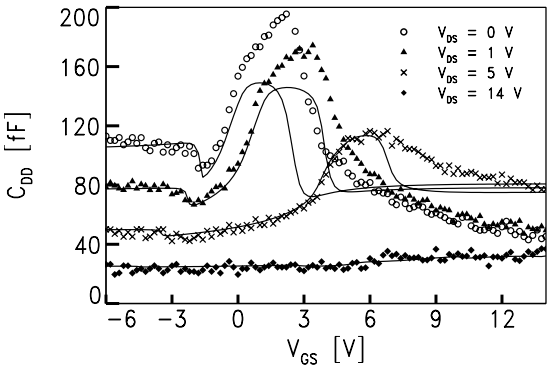

Figure 6: Measured (symbols) and modelled (solid lines) capacitance value $C_{\rm DD}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 0$, 1, 5 and 14 V, for $W_{\rm mask} = 50$ μm and $L_{\rm PS} = 5$ μm.

In Figure 7 the cut-off frequency $f_{\rm T} = |Y_{\rm DG}/Y_{\rm GG}|$ as function of the gate bias is plotted. We observe that the cut-off frequency agrees well with the modelled ones.

3 NEW DEVELOPMENTS

3.1 Quasi-Saturation

In MOS Model 20 the assumption made is that velocity saturation occurs only in the channel region. For short drift region devices, however, saturation may occur in the drift region, which is also known as quasi-saturation. To take quasi-saturation into account, the drift region current needs to be extended with velocity saturation. To that end, the electron mobility $\mu^{\rm dr}$ of the drift region is taken as

$$\mu^{\rm dr} = \frac{\mu_{\rm eff}}{1 + \theta_3^{\rm dr} V_{\rm DDi}} \qquad (3)$$

where $\mu_{\rm eff}$ is the effective electron mobility including the reduction due to the vertical electrical field, and $\theta_3^{\rm dr} = \mu_{\rm eff}/(L_{\rm D} v_{\rm sat})$, with $L_{\rm D}$ the length of the drift region, and $v_{\rm sat}$ the saturated drift velocity of electrons.

In Figure 3.1 the influence of $\theta_3^{\rm dr}$ on the drain current is demonstrated. For $V_{\rm GS} = 6$ V, velocity saturation occurs in the channel region, and hardly any influence of $\theta_3^{\rm dr}$ is observed. For $V_{\rm GS} = 12$ V, however, velocity saturation occurs in the channel region for $\theta_3^{\rm dr} = 0$ and 0.4 1/V, but it occurs in the drift region for $\theta_3^{\rm dr} = 0.8$ 1/V.

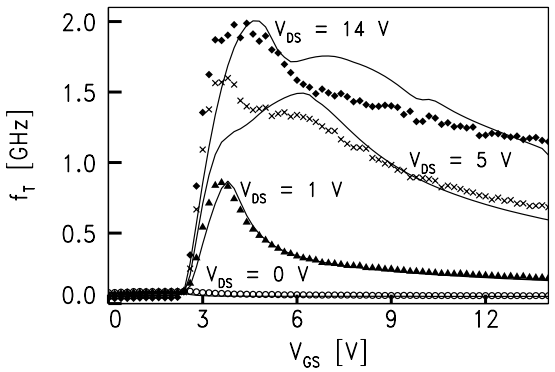

Figure 7: Measured (symbols) and modelled (solid lines) cut-off frequency $f_{\rm T}$ versus $V_{\rm GS}$, for $V_{\rm DS} = 0$, 1, 5 and 14 V, for $W_{\rm mask} = 50$ μm and $L_{\rm PS} = 5$ μm.

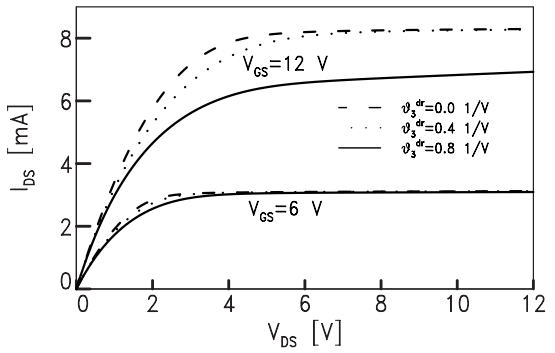

Figure 8: Simulated drain current $I_{\rm DS}$ for different values of the drift region saturation parameter $\theta_3^{\rm dr}$, for $V_{\rm GS} = 6$ and 12 V, and $V_{\rm SB} = 0$ V.

3.2 Capacitance Modelling of Laterally Non-Uniform MOS Devices

In an LDMOS device two kinds of lateral non-uniformity can be distinguished: the first one due to the transition from a p-type channel region to an n-type drift region, and the second one due to the diffused doping profile in the channel region. For laterally non-uniform MOS devices in general, we have found a new, fundamental result for the correct way of capacitance modelling [17]. For a detailed investigation we refer to [17]. Below, the new result is explained briefly.

For laterally uniform MOS devices, charges can be assigned to each terminal, where the source- and drain charge are obtained from the inversion charge using the well-known Ward-Dutton charge partitioning scheme [16]. Thanks to the existence of the nodal charges, the capacitances satisfy (1). As a result, if a nodal charge Q_i exists, then

$$(2\delta_{ik} - 1)\partial C_{ij}/\partial V_k = (2\delta_{ij} - 1)\partial C_{ik}/\partial V_j \qquad (4)$$

holds, and the integral $q_{\mathrm{c},\,i}$ of the charging current through terminal i for a closed voltage cycle in time equals zero, i.e.

$$q_{\mathrm{c},i} \equiv \oint [I_i(t) - I_{\mathrm{T}}(t)]\,\mathrm{d}t = 0, \qquad (5)$$

where I_i is the total current through terminal i and I_{T} is the transport current.

For laterally *non*-uniform MOS devices, however, implications (4) and (5) of the existence of a nodal drain- and source charge model are *not* true: In Figure 11 we observe that the integrals of the charging current for several closed voltage cycles in time through the bulk- and gate terminal indeed exactly equals zero. The integrals of the charging current through the drain- and source terminal, however, are not equal to zero. In Figure 9 we observe that $-\partial C_{\mathrm{GG}}/\partial V_{\mathrm{D}}$ exactly equals $\partial C_{\mathrm{GD}}/\partial V_{\mathrm{G}}$, while in Figure 10 we observe that $\partial C_{\mathrm{DG}}/\partial V_{\mathrm{D}}$ is not equal to $-\partial C_{\mathrm{DD}}/\partial V_{\mathrm{G}}$. Thus, (4) and (5) do not hold for the drain- and source terminal of laterally non-uniform MOS devices. As a result, *no* terminal drain- and source charge model exists for these devices. A terminal gate- and bulk charge model, on the other hand, does exist (provided that the leakage currents through the gate can be neglected).

The consequence is that for a compact LDMOS model, instead of a nodal charge model, a capacitance model needs to be derived. In [17] a method is demonstrated to incorporate a capacitance model into circuit simulators, which are based on nodal charge models.

A first step towards a capacitance model for an LDMOS device is obtained by taking a uniformly p-type doped channel region (thus neglecting the diffused doping profile) in series with an n-type doped drift region. By a small-signal analysis the capacitances of such LDMOS device can be written in terms of the capacitances

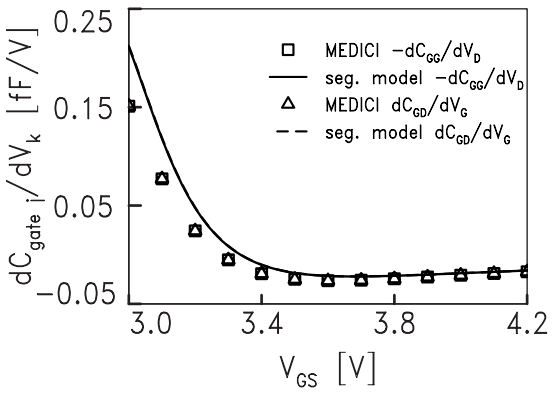

Figure 9: Partial derivatives of gate-related capacitances for a laterally non-uniform MOSFET with diffused doping profile$N_A(x) = N_{A0}\exp(-D(x/L)^2)$, $D = 2.78$, at $V_{\mathrm{DS}} = 0.5$V. Symbols represent MEDICI simulations and lines a segmentation model.

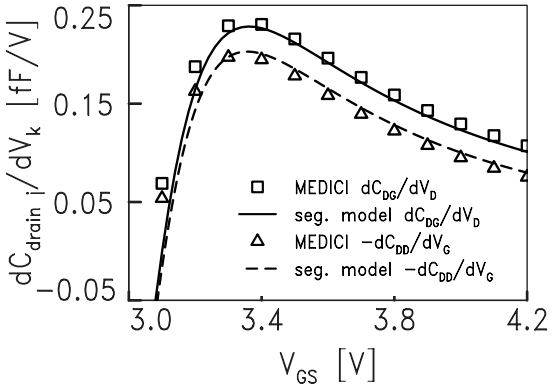

Figure 10: Partial derivatives of drain-related capacitances for a laterally non-uniform MOSFET with diffused doping profile $N_A(x) = N_{A0}\exp(-D(x/L)^2)$, $D = 2.78$, at $V_{\mathrm{DS}} = 0.5$V. Symbols represent MEDICI simulations and lines a segmentation model.

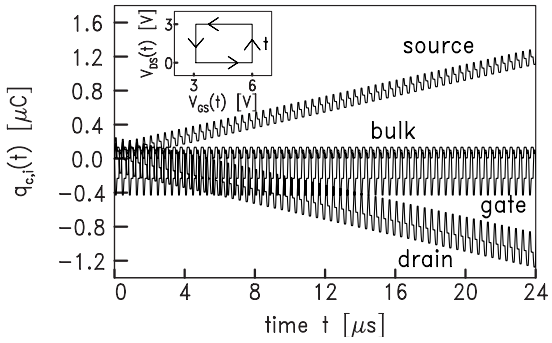

Figure 11: Integral of the charging current through the drain- source-, gate- and bulk terminal of a laterally non-uniform MOSFET with diffused doping profile $N_A(x) = N_{A0}\exp(-D(x/L)^2)$, $D = 2.78$, for 60 closed voltage cycles in time (according to the inset, 0.4μs cycle time), obtained using the segmentation model.

and conductances of the channel region and those of the drift region [18]. For instance, at $V_{\rm DS} = V_{\rm SB} = 0$ V, the capacitance $C_{\rm DG}$ of the LDMOS device is given by

$$C_{\rm DG} = \frac{g_{\rm DS}^{\rm dr}}{g_{\rm DS}^{\rm ch} + g_{\rm DS}^{\rm dr}} \left(C_{\rm DG}^{\rm ch} + C_{\rm SG}^{\rm dr} \right) + C_{\rm DG}^{\rm dr}, \qquad (6)$$

where $g_{\rm DS}$ is the output conductance. The superscript "ch" refers to the channel region and "dr" to the drift region.

To evaluate the impact of the recent findings [17] in capacitance modelling of laterally non-uniform MOS devices, we investigate the capacitance model of MOS Model 20 (which is derived from its nodal charge model). To that end, we compare $C_{\rm DG}$ of MOS Model 20 at $V_{\rm DS} = V_{\rm SB} = 0$ V (where the modified Ward-Dutton charge partitioning scheme applies) with the one obtained from (6). Here, the dc-current expressions of MOS Model 20 for the channel region and the drift region are used to determine the conductances of each region. In Figure 12 we observe that the capacitance according to Equation (6) slightly better reflects the shape of the measured one than the capacitance of MOS Model 20 does. But, since the two capacitance values are quite close, the modified Ward-Dutton charge partitioning scheme seems to provide a practical way to model the capacitances of an LDMOS device. Notice that in both models, the deviation with measurements is caused by the neglect of the diffused doping profile in the channel region.

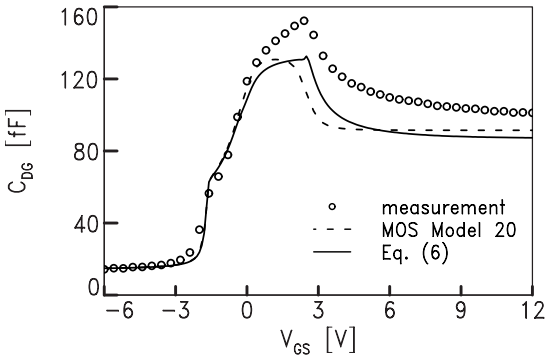

Figure 12: Comparison of $C_{\rm DG}$, obtained with MOS Model 20 (dashed line) and from Eq. (6) (solid line), in relation to measurements (symbols), for $V_{\rm DS} = 0$ V, $W_{\rm mask} = 50$ μm and $L_{\rm PS} = 5$ μm.

4 SUMMARY

Various modelling approaches for LDMOS devices have been discussed. Characterisation results for the surface-potential-based compact LDMOS model called MOS Model 20 have been presented. By taking into account the current through the channel region as well as through the drift region, MOS Model 20 provides an accurate dc-description in all operating regimes. The nodal charge model of MOS Model 20, in which the lateral non-uniformity is taken into account via a modified Ward-Dutton charge partitioning scheme, yields an adequate description of the capacitive behaviour, even in view of the fact that for laterally non-uniform MOS devices no nodal drain- and source charge model exists. In the future, developers of compact models for LDMOS devices should consider the derivation of capacitance models instead of charge models. Finally, a method to incorporate quasi-saturation in MOS Model 20 has been evaluated.

REFERENCES

[1] R.S. Scott, G.A. Franz and J.L. Johnson, *IEEE Trans. Power Electron.*, **6**, pp. 192-198, 1991.

[2] J. Jang, T. Arnborg, Z. Yu and R.W. Dutton, *Proc. SISPAD*, pp. 15-18, 1999.

[3] N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A.M. Ionescu and R. Gillon, *Proc. SISPAD*, pp. 203-206, 2002.

[4] A.C.T. Aarts, M.J. Swanenberg and W.J. Kloosterman, *Proc. SISPAD*, pp. 246-249, 2001.

[5] J. Victory, C.C. Mc Andrew, R. Thoma, K. Joardar, M. Kniffin, S. Merchant and D. Moncoqut, *Proc. SISPAD*, pp. 271-274, 1998.

[6] Y. Kim, J.G. Fossum and R.K. Williams, *IEEE Trans. Electron Devices*, **38**, pp. 1641-1649, 1991.

[7] Y. Chung and D.E. Burk, *Proc. ISPSD*, pp. 340-345, 1995.

[8] M.Y. Hong and D.A. Antoniadis, *IEEE Trans. Electron Devices*, **42**, pp. 1614-1622, 1995.

[9] Y. Chung, *IEE Proc. Circuits Devices Syst.*, **147**, pp. 219-227, 2000.

[10] C.M. Liu, F.C. Shone and J.B. Kuo, *Proc. ISPSD*, pp. 321-324, 1995.

[11] Y. Subramanian, P.O. Lauritzen and K.R. Green, *Proc. Modeling and Simulation of Microsystems*, pp. 284-288, 1999.

[12] N. D'Halleweyn, L. Tiemeijer, J. Benson, M. Swanenberg and W. Redman-White, *Proc. ISPSD*, pp. 291-294, 2001.

[13] A.C.T. Aarts and R. van Langevelde, *Proc. ESSDERC*, pp. 455-458, 2002.

[14] www.semiconductors.philips.com/Philips_Models.

[15] A.C.T. Aarts, N. D'Halleweyn and R. van Langevelde, *IEEE Trans. Electron Devices*, submitted.

[16] S.-Y. Oh, D.E. Ward and R.W. Dutton, *J. Solid-State Circuits*, **15**, pp. 636-643, 1980.

[17] A.C.T. Aarts, R. van der Hout, J.C.J. Paasschens, A.J. Scholten, M. Willemsen, and D.B.M. Klaassen, *IEDM Tech. Digest*, pp. 751-754, 2004.

[18] C. Liu and J. Kuo, *IEEE Trans. Electron Devices*, **44**, pp. 1117-1123, 1997.