

Novel Approach to Circuit Board Testing

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ABSTRACT

This paper describes research and development efforts in the application of nanoscale sensors to implement an original method for bed-of-needles testing for printed circuit boards testing. This approach performs functional testing that eliminates the need to have a pre-existing model of a circuit board while automating much of the development process. The general concept involves creating arrays of nanoscale sensor probes, using molecular electronics for incorporating test instruments and computing logic for test interpretation directly into a pod consisting of multiple nails, and distributing these pods across the face and back of a circuit card using a contact fixture. The resulting test approach exhibits massive parallelism combined with extremely compact size that facilitates novel testing approaches not possible with current generation or planned test equipment. In consequence, many existing limitations are expected to be overcome with test speed and accuracy significantly improved.

Keywords: carbon nanotube electronics, nanoscale sensors, circuit board testing

1 INTRODUCTION

A problem exists in circuit board testing whereby advances in IC and printed circuit board technology have surpassed existing capabilities with respect to test hardware and software. The physical size of electronic components and ICs has decreased over time, making it more and more difficult to access component parts and suitable test points. Additional issues that are problematic for today's test approaches include the increased performance and complexity of today's ICs, degradation in circuit performance due to I/O and signal path loss, noise insertion from long signal paths between unit under test (UUT) and automatic test equipment (ATE), and increased difficulty in obtaining comprehensive models of circuit components. Also, the increased complexity of circuitry on circuit cards results in longer development times and greater dependency upon human intervention in test program development. So-called Automatic Test Program Generators (ATPGs) are becoming less and less automatic. Furthermore, in

concordance with Moore's Law, the doctrine estimating that computing power doubles every 18 to 24 months, it is expected that by year 2015 the dimensions of ICs within boards will require new testing methodologies as the scale of their discrete devices will reach sub-micron dimensions resulting in an increased amount and density of I/O pins [1]. After evaluating alternatives (e.g. non-comprehensive boundary scan techniques), we took a second look at the application of new technologies and tools to existing test methods to see whether the potential exists to improve in their implementation. Second, we examined this approach to determine whether these improved techniques could supplement boundary scan and other existing and future test approaches.

The result of this investigation is the conceptualization of a test methodology where we bring nanoscale probes and measurement equipment (e.g., logic state detection, DC, AC, frequency, pulse, etc.) directly to the IC and circuit board signal path. This approach eliminates the potential for all path loss compensation and interference injection problems, and dramatically reduces timing problems, especially those typically encountered during digital testing. In addition, this approach also reduces the problem of a lack of test points since it establishes virtually thousands of test points across the top and bottom of the circuit board.

2 TEST SYSTEM CONCEPT

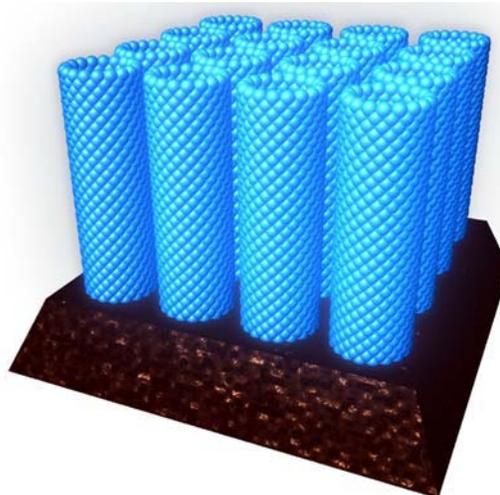


Figure 1: Individual Sensor Architecture

Figure 1 provides an illustration of a sensor pod architecture including the probe elements chemically bound to sensor circuits in the sensor pod base, as well as in the substrate of the next higher assembly. This combination of sensor filaments, interconnections, and sensor circuitry (where applicable) physically interconnect with the UUT surfaces (e.g., IC pin, circuit path, etc.) from which measurements or other actions are to be made.

Individual sensors are clustered into pods, each having an entire suite of measurement equipment. Sensor pods, in turn, form instrument clusters that combine to create the entire nanosensor pin bed.

During testing, the circuit card is placed between two nanosensor pin beds, whereby the top and bottom surfaces of the card are bathed in sensors that make contact with IC pins and circuit paths.

This approach culminates in the development of a nanosensor pin test system, illustrated in Figure 2. This system is comprised of a test fixture consisting of two nanosensor pin bed assemblies between which the UUT resides, a Test Computer for test program execution, a PXI-bus test fixture facilitating I/O between the NanoSensor Pin Bed assemblies and the test computer, appropriate interface cabling and connectors, and other ATE assets required to exercise the UUT at the card edge connectors and boundary scan port, if available.

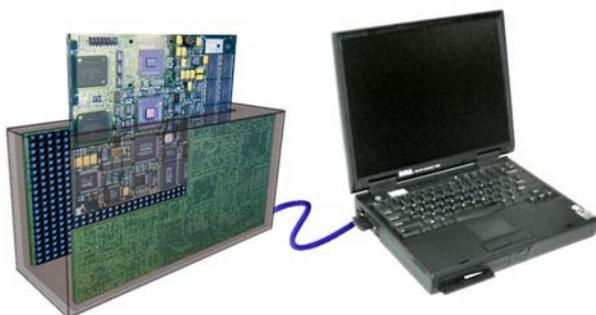


Figure 2: Nanoscale Sensors Applied to Both Sides of a UUT During a NanoSensor Pin Test System

Due to their extremely small size, one IC pin or circuit board signal path will extend across multiple sensor pod clusters, ensuring that multiple and redundant measurements may be taken to improve measurement reliability. The test architecture depicted here presents the nanosensor pin beds serving mainly as just an interface device. However, our vision anticipates gradual evolution from the concept of test fixture with molecular circuitry performing just supplementary functions of data collection and enhancing the capabilities of the PXI (or PC) system to the fully independent (stand-alone) arrangement comprised of molecular-test-system-embedded nanosensor pin beds.

The paragraphs that follow describe the challenges of implementing the above-presented concept. Creating the nanosensor-pin test system calls for exploring the truly interdisciplinary field of molecular electronics, which brings together elements of chemistry, physics, and

electrical engineering. Therefore, to allow for a broader picture of our idea, before describing our current research progress, we provide background regarding the functionality anticipated to result from our approach.

3 NANOSENSOR-PIN TEST SYSTEM DESIGN AND DEVELOPMENT

The best illustration of our approach is the comparison of our design with well-known concept of bed-of-nails fixtures. We first describe our idea to update this traditional approach where we increase probe density by several orders of magnitude, in addition to placing the measurement instruments directly at the probe point. We follow this discussion with details regarding the methods we use to design and fabricate the nanoscale probe elements and chemically synthesize the electronic circuitry comprising the measurement equipment.

3.1 Concept Background

The first machines using universal fixturing were introduced to the PCB industry in the early '80s. Sometimes called "bed-of-nails" fixtures, the universal grid was a revolution. In 1980, less than 10% of the bare boards produced in the U.S. were electrically tested. In 1988 more than 75% were tested. Today the percentage of boards tops 95% [2]. The use of fixtures for early-dedicated machines was expensive and laborious. Hence, their application was only justified for large volume. A universal grid is what the name implies. It is populated with test points, originally placed on 0.100, or 100 points/in², grids. The number of test points, then, is a matter of the desired physical size and the cost. An 18 x 24 grid contains 43,200 test points. When used with a test fixture interface, the number of test points actually in use is only the number required for the board to be tested. To contrast this technology with our approach, we expect to achieve grid density in excess of 10,000+ points/in², with densities exceeding 35,000 points/in² possible.

To carry out the test it is necessary to gain access to each node on the board. The most common way of achieving this is to generate a "bed of nails" fixture. The board is held in place accurately by the fixture and pulled onto test-fixture pins that make contact with connectors on the board. The board may either be pulled down under the action of a vacuum or it may be achieved mechanically [3].

Because current generation bed-of-nails testers are relatively complex and expensive, this type of testing is most suited to situations requiring testing a large volume of circuits and circuit boards quickly. Furthermore, it will serve to distribute high cost over many tested circuits, and minimizes access requirements to prime ATE assets [2].

3.2 Design Considerations

The following represents our design considerations for the fabrication of all the elements that will constitute the nanosensor-pin test system.

Sensor Pod Cluster

Pod cluster development is divided into two general parts. The first part of the research pertains to the fabrication of the pod cluster panel itself including conductive pod bases and connections providing individual addressing of each pod, as well as carbon nanotube arrays formed on top of the pod bases. The second general part describes the formation of the nano-scale sensor circuits to be created at the back of each pod cluster panel.

The sensor pod clusters consist of a number of individually addressed pods connected to a sensor circuit situated at the back side of the sensor pod cluster panel. The bases of the pods as well as the individual connections are expected to be built using either ink-jet printing-produced conductive-polymer circuitry or metallic circuitry fabricated with use of photolithographic techniques. The production of a mesh of the metallic pod bases on silicon substrate will be relatively straightforward, and we anticipate utilizing previously verified sources of photolithography manufacturing in order to accomplish this task [3].

For the production of the sensor pods, we have initially selected carbon nanotubes (CNT) over other types of materials due to their unusual electrical and mechanical properties. Carbon nanotubes exhibit both extraordinary durability and flexibility allowing for multiple usages of created pin beds for various types of circuit boards. Moreover, CNTs are the most studied of all the nanostructures and the most promising for obtaining near term practical results in electronics and electronic devices.

Sensor Circuits

Sensor circuits are to be produced on the backside of the earlier described pod clusters. Due to the relatively small area on which we will have to create fairly complex electronic devices, we predict that in addition to traditional electronic devices, other technologies will have to be applied including nano-scaled molecular electronics.

We are currently exploring methods of creation of simple molecular electronic logic devices, which can then be combined into more sophisticated systems. The molecular systems will include polyphenylene-based devices synthesized using organic chemistry methodologies developed by James Tour [4]. The basic materials for construction of those molecular electronics are Tour wires, which are polyphenylene-based molecules with different substituents incorporated into their structure. Using these structures as simple building blocks, we can fabricate discrete electronic devices including rectifier diodes, tunneling diodes, or transistors. These devices, in turn, can be further combined to create logic gates.

System Software

The primary requirement is the creation of software that will control the nanosensor pin test system hardware, as well as process sensor measurements to create and execute a resulting test program in a LabView environment. The system software will have two primary components that are run sequentially. The first component is the pattern analysis software, whose job is to determine which nanosensor pins of the test bed are relevant to the test of a particular UUT and removes the rest from the test configuration. It also identifies areas of continuity that are representative of IC pins and circuit paths. The second component is the test analysis software itself, comprised of the software used to create a test program through semi-automated means, and the resulting executable test program software hosted on the ATE.

The pattern analysis software examines continuity measurements reported by sensor pods on both NanoSensor Pin Bed assemblies to detect patterns of connectivity illustrative of IC pins and circuit paths. Due to their extremely small size, numerous sensor pod clusters will span the distance of individual IC pins and circuit paths. Areas of continuity on a circuit board represent metallic connections through which electrical signals flow with minimal resistance, i.e., IC pins and circuit paths. Areas where electrical signals do not flow include IC packages and other electronic components, as well as blank areas on a circuit board. Establishment of such areas of continuity on the UUT will effectively result in the creation of a netlist.

This software module is anticipated to use a continuity measurement probe identified in the system requirements specification, consisting of probe elements and circuitry that apply extremely low power stimulus and/or measure very low power signals to determine if a shorted condition may exist between two or more sensor pods through a UUT surface (IC pin, circuit path, etc.). A positive reading would mean two or more sensor pod interfaces are located on the same IC pin or circuit board conductor.

Patterns of continuity will be identified through examination of the measurements obtained from these probes. Positive measurements will be tagged and configured to an active state. Sensor pod clusters that do not depict areas of continuity will be configured to an inactive state. Thus, only the remaining active sensor pod clusters are of interest for the performance of UUT testing and will be queried for this purpose. This step significantly reduces the search space and computational requirements for the test analysis software.

Further processing will then take place to identify specific paths and IC pin connections. This may be accomplished through an automated process in the event a netlist is available from an independent source. In this case, we would be able to compile a list of total connections on a UUT as well as a list of exposed connections. In the event this is not possible, the user may interactively designate

connectivity elements presented through a graphical user interface.

Upon completion of sensor pod cluster configuration and netlist generation, the pattern analysis software will compile a record of the test environment for the UUT within which the test analysis software will create a test program set.

For test program set generation, an initial stimulus input set consisting of a uniform distribution of test patterns will be applied. The measurements obtained from the test pods for each input stimulus pattern will be collected. Test patterns will be iteratively generated based on a perturbation function determined from the correlation between the set of input patterns and the resulting measurements. Inconsistent results will appear as singularities in the output measurements, such as a curve of current vs. voltage. The process is similar to a feedback based Monte-Carlo simulation approach, in which an estimate of the joint distribution of a large number of variables can be determined by obtaining samples at intervals on the distribution curve. For traditional Monte-Carlo simulation, values are randomly generated for the variables of interest in order to simulate a model. However for our approach, no simulation is needed, since the actual measurements will be taken for each input stimulus.

4 CONCLUSIONS

Much of the technology identified within this paper is graduating from the theoretical to the practical domain. Improvements in tools such as the atomic force microscope and scanning electron microscope, as well as recent advances in the development of nanoscale manipulation tools, have afforded us unprecedented visibility and capability in directly effecting research at the atomic level – even to the extent of the physical manipulation of individual atoms. As IC technology continues to shrink into the nanometer realm, our nanosensor-pin testing paradigm presents a modern cutting-edge test method, and may one day be the platform through which future generations of test methodologies that address the sub-micrometer dimensions are based.

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