Modeling of Saturation-Region Characteristics of Nanoscale Double-Gate MOSFETs

J. G. Fossum and S. Chouksey

Department of Electrical and Computer Engineering
University of Florida
Gainesville, FL 32611-6130, U.S.A.

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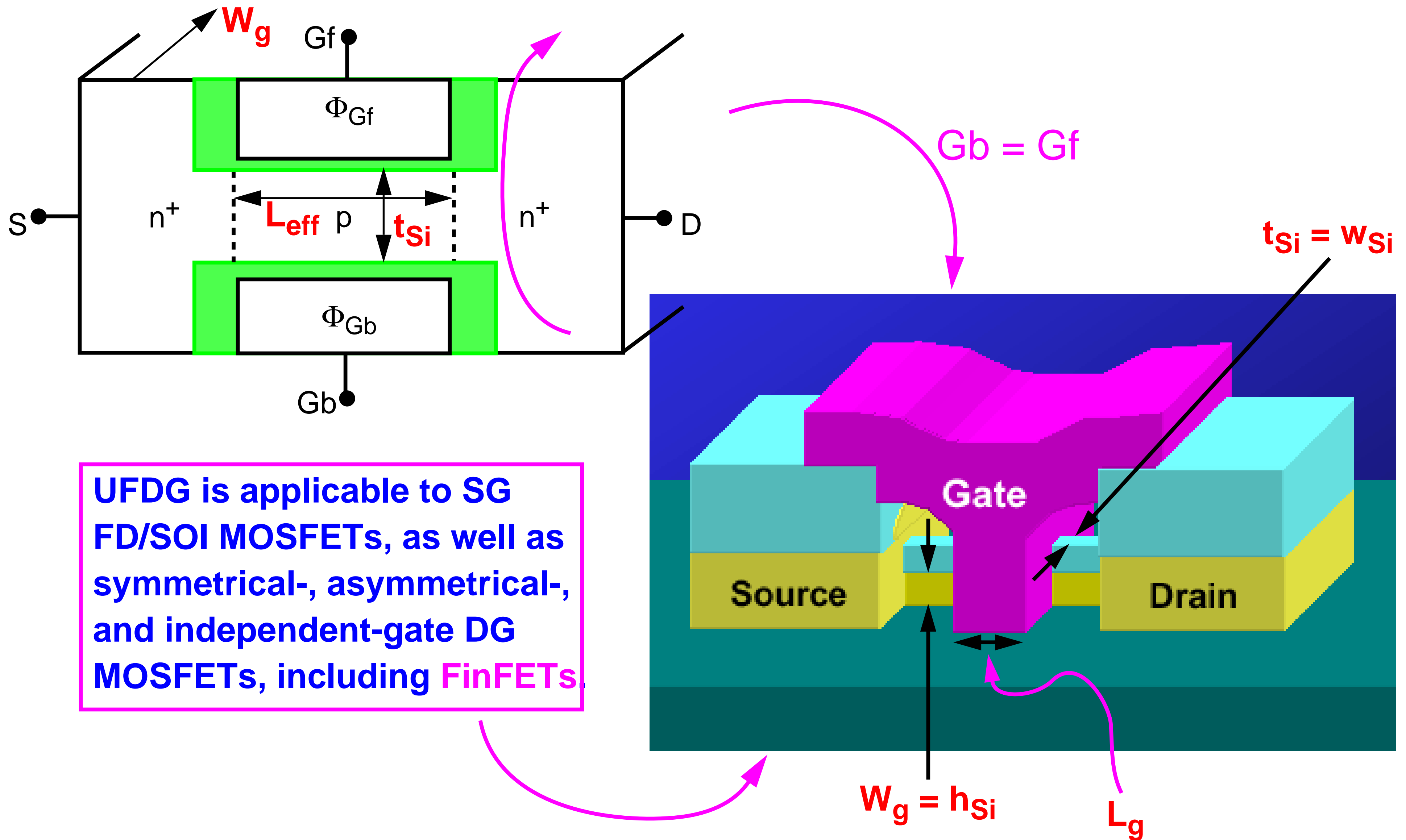
Outline

* UFDG Overview
* High Carrier Mobility in DG FinFETs
* Carrier Velocity Overshoot / Quasi-Ballistic Transport
* Drain-Induced Charge Enhancement (DICE)
* Summary

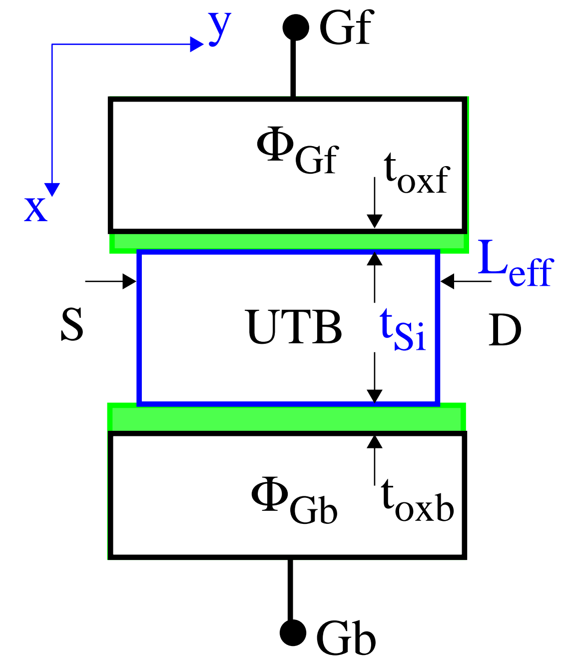
UFDG: A Process/Physics-Based Predictive Compact Model Applicable to Generic UTB DG MOSFETs



Short-Channel Effects Modeling in UFDG

The 2-D Poisson equation, for weak inversion,

$$\frac{\partial^2\phi}{\partial x^2} + \frac{\partial^2\phi}{\partial y} \cong \frac{qN_B}{\varepsilon_{Si}} \quad ,$$



is solved in the (rectangular) FD body/channel (UTB) region, defined by t_{Si} and L_{eff} ($\neq L_g$), by assuming

$$\phi(x, y) \cong \alpha_0(y) + \alpha_1(y)x + \alpha_2(y)x^2$$

in Poisson, and applying the (four) boundary conditions (including surface-state charge at both interfaces). The derived potential, with the QM shift, defines the integrated (in x-y, over t_{Si}) inversion-charge density (Q_{ch}) and an effective channel length ($< L_{eff}$) for predominant diffusion current (in y) averaged over t_{Si}, and thus accounts for:

* **S/D charge (impurity and/or carrier) sharing [$V_t(L_{eff})$ & $S(L_{eff})$]** ,
* **DIBL (throughout UTB) [$\Delta V_t(V_{DS})$]** .

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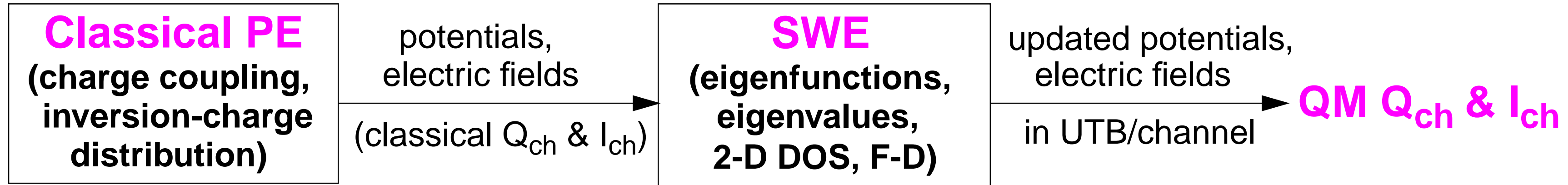
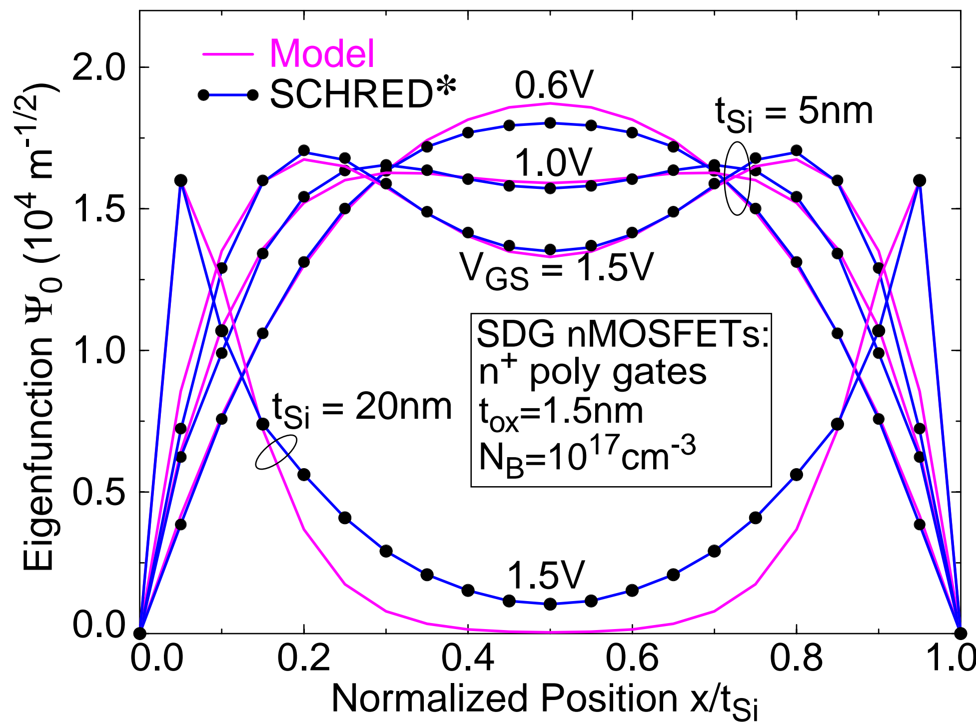
Quantization Effects Modeling in UFDG

UFDG is actually a Compact Poisson-Schrödinger Solver:





1-D SWE analytical solution is derived using a variational approach, then coupled to PE and $Q_{ch}(V_{GfS}, V_{GbS})$ via Newton-Raphson iteration, all with dependence on t_{Si} and Si orientation, as well as E_x.

UFDG is $\phi(x)$- and $\Psi(x)$-based, not merely surface potential-based!

*1-D numerical PE-SWE solver [D. Vasileska and Z. Ren, Purdue Univ., W. Lafayette, IN, Feb. 2000].

UTB Carrier Transport Modeling in UFDG

Effective Carrier Mobility

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_{ph}} + \frac{\theta}{\mu_{sr}}$$

$\mu_0 \Leftarrow$ **Mobility in thick-t_{Si} device at low E_x, or a tuning parameter defined by Coulomb scattering that does not depend on E_x nor t_{Si}.**

$\mu_{ph} \Leftarrow$ **Phonon scattering, QM-based, dependent on both E_x and t_{Si}.**

$\mu_{sr} \Leftarrow$ **Surface-roughness scattering, dependent only on E_x (for viable t_{Si} > 4nm).**

θ: **A tuning parameter to account for uncertainty in the surface roughness (≅1 nominally).**

Quasi-Ballistic and Ballistic Transport

Quasi-ballistic via carrier velocity overshoot, dependent on carrier temperature (T_c) along the channel:

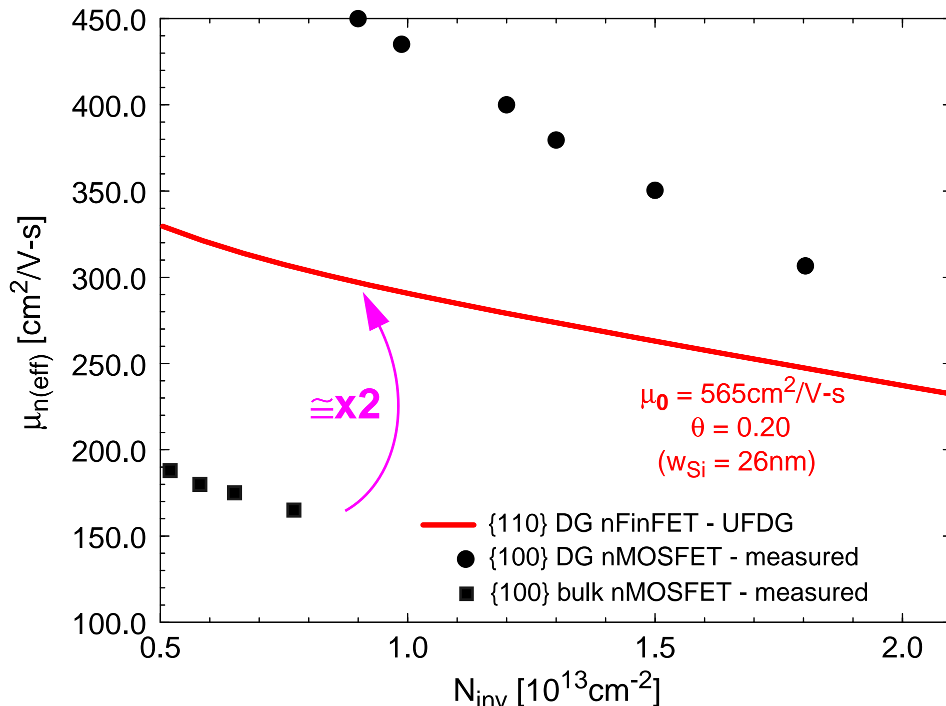
$$v_{sat(eff)} = \Delta L\left[\int_{\Delta L} \frac{1}{v(T_c(y))} dy\right]^{-1} > v_{sat} ,$$

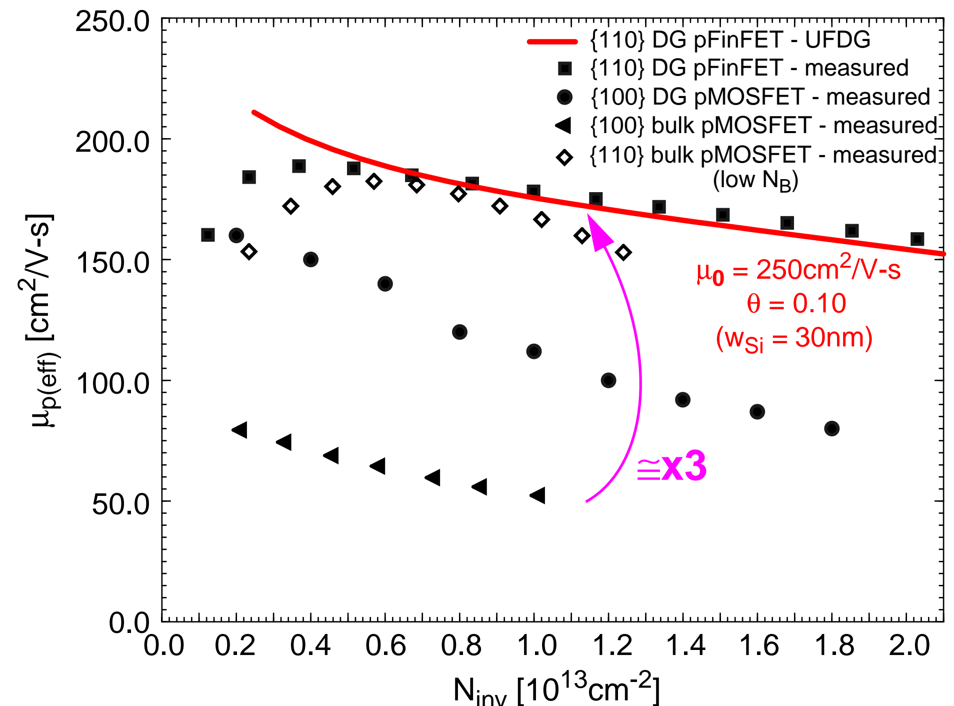
with only one tuning parameter: VO (≅1 typically).

Ballistic via the ballistic-limit current characterized by Natori's QM-based model for thermal injection velocity at the source, summed over important subbands:

$$I_{lim} = W_g \sum_j qN_{inv(j)} v_{inj(j)} .$$

UFDG Calibrations to Contemporary DG FinFETs





The high carrier mobilities are due to mainly to low transverse electric field stemming from the two gates and the undoped UTB/channel. They tend to yield beneficial velocity overshoot and DICE in the saturation region of nanoscale DG MOSFETs, which is not the case in conventional, single-gate highly doped (N_B >10^{18}cm^{-3}) MOSFETs.

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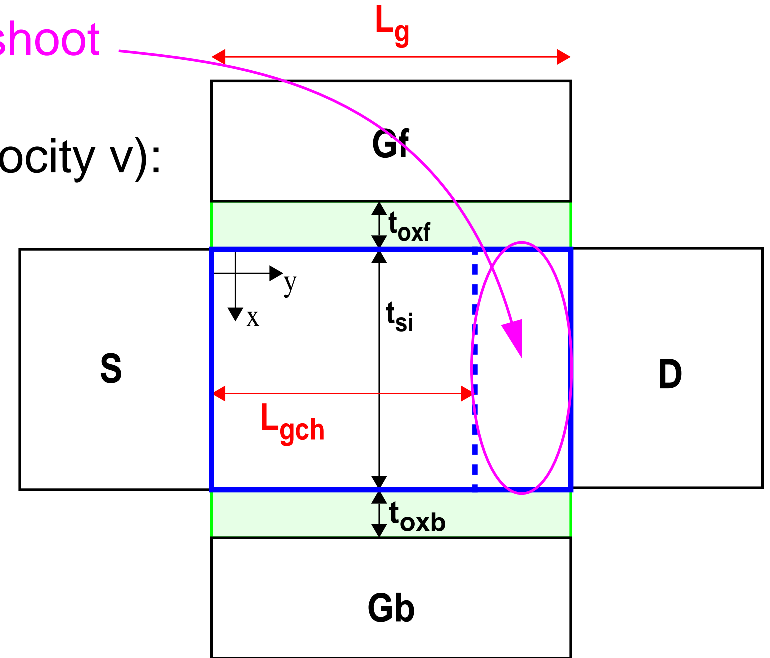
Carrier Velocity Overshoot Modeling in UFDG

Near drain, high E_y, $dE_y/dy \Rightarrow T_c(y)$ lags $E_y(y) \Rightarrow$ overshoot



1st-order BTE moment (for average momentum, or velocity v):

$$v = \mu_{eff}(E_y)E_y\left(1 + \frac{k_B}{qE_y}\frac{dT_c}{dy}\right). \quad (1)$$

2nd-order BTE moment (for average energy, or T_c):

$$\frac{d}{dy}(T_c(y) - T) + \frac{(T_c(y) - T)}{(5v\tau_w/3)} = \frac{2qE_y(y)}{5k_B}. \quad (2)$$

The moments (1) and (2) characterize $T_c(E_y)$, which, when combined with familiar steady-state $\mu_{eff}(E_y)$, and $E_y(y)$ from UFDG formalism, yields v(y). Then, defining a bias-dependent

$$v_{sat(eff)} = \Delta L\left[\int_{\Delta L}\frac{1}{v(y)}dy\right]^{-1} > v_{sat}$$

based on the transit time across $\Delta L = L_g - L_{gch}$ renders a physical compact model for the overshoot (a beneficial short-channel effect), or quasi-ballistic transport.

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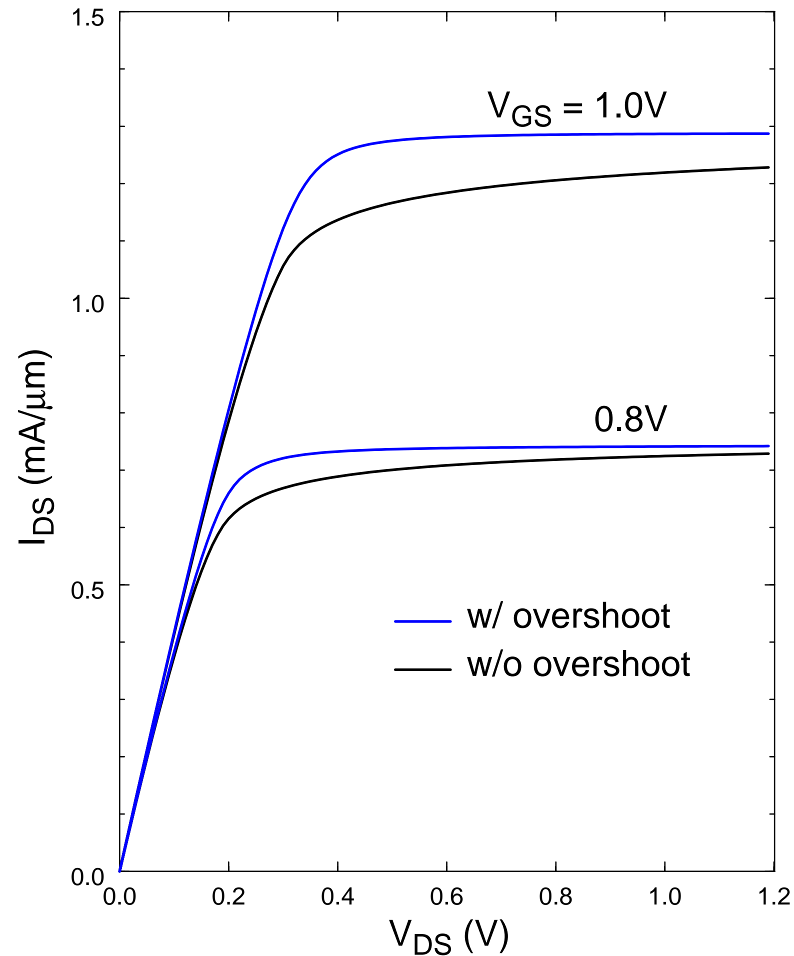
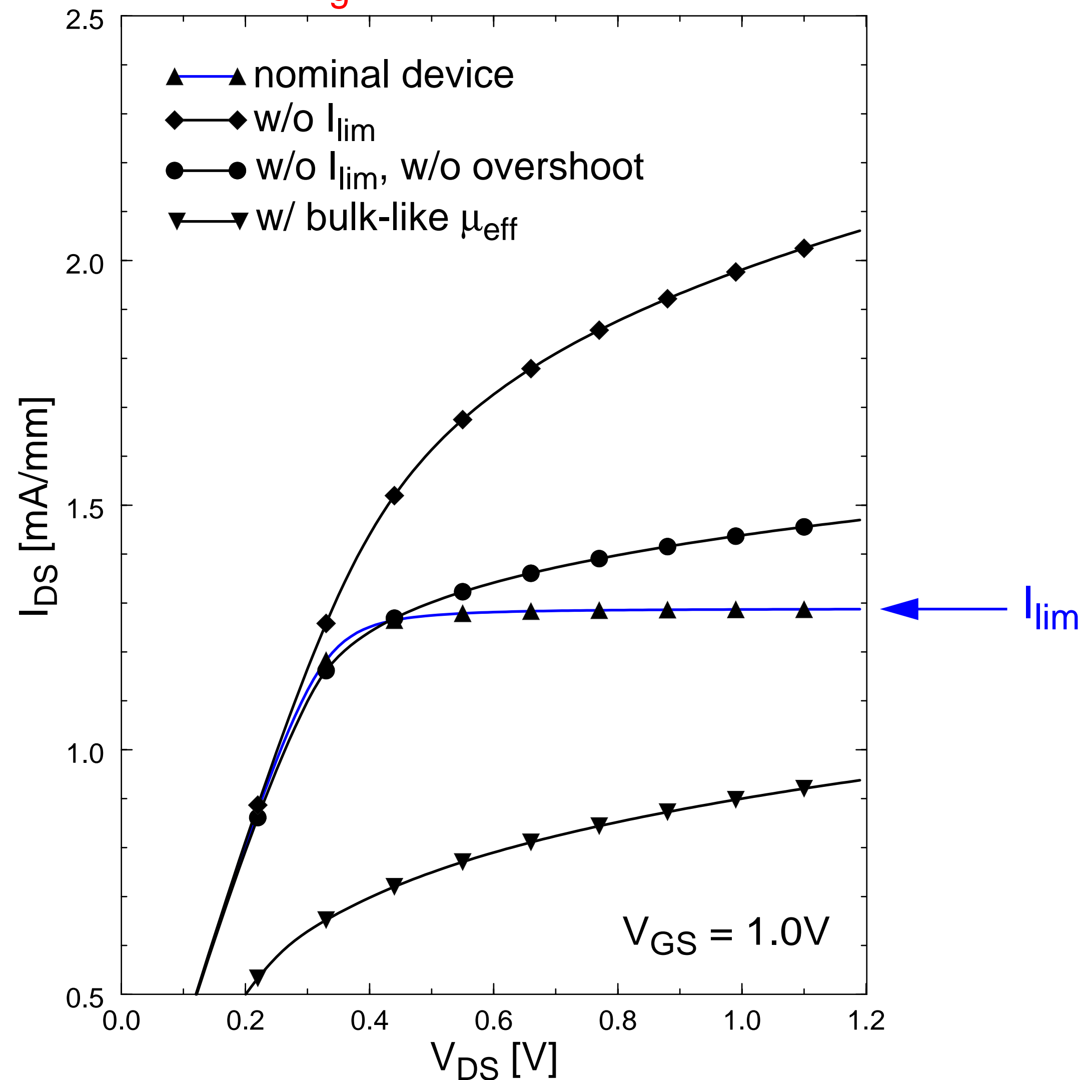
Nanoscale DG MOSFETs, with high μ_{eff}, should show substantive carrier velocity overshoot, which could result in near-ballistic transport:

UFDG: L_g = 18nm SDG nMOSFET; $t_{oxf} = t_{oxb} = t_{ox}$ = 1.0nm, t_{Si} = 9nm, midgap gate



The benefit of the overshoot is restrained by the ballistic-limit current (I_{lim}) ...



Bulk-like μ_{eff}, severely limited by impurity scattering and enhanced surface-roughness scattering due to higher E_x, limits the benefit of overshoot and prevents ballistic transport.

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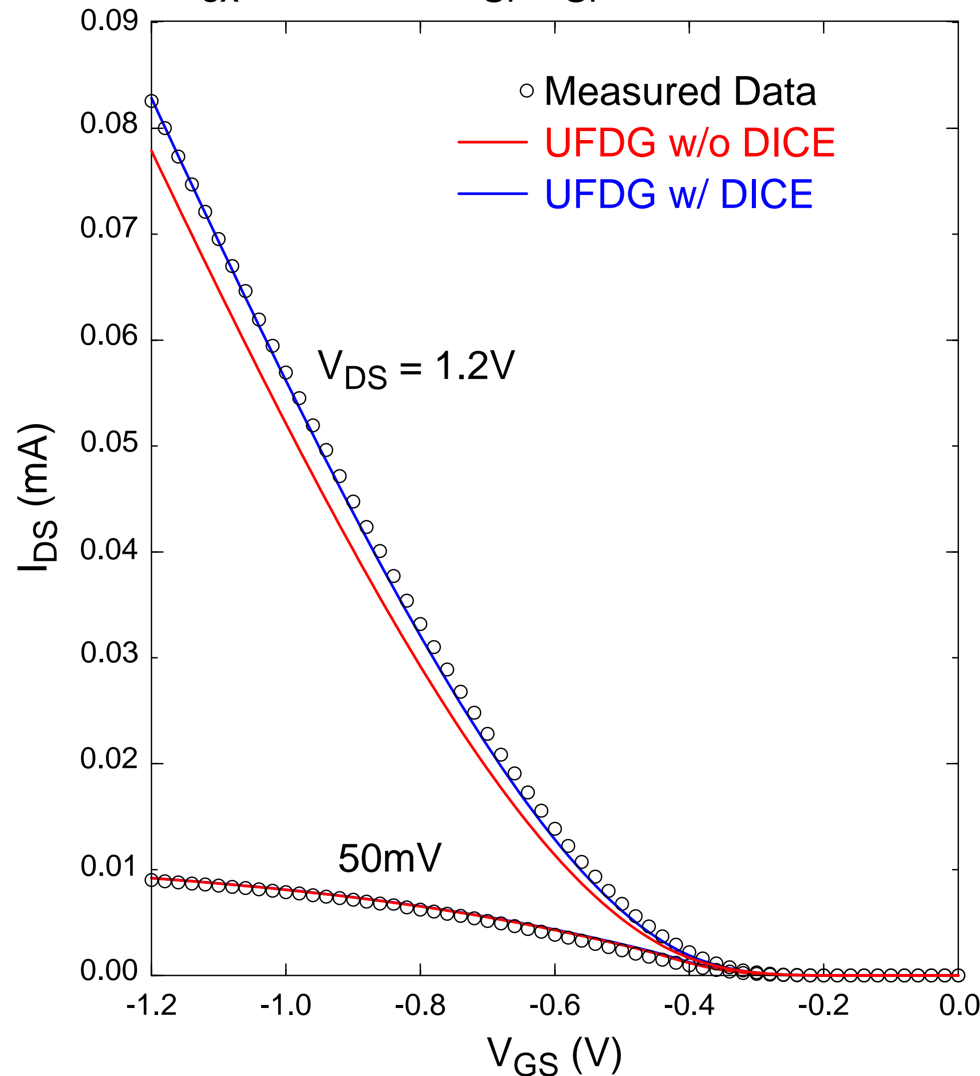
UFDG Calibrations to Nanoscale DG FinFETs ⇒ **DICE**

L_g = 60nm DG pFinFET; t_{ox} = 1.5nm, h_{Si}/w_{Si} = 100nm/17nm, near-midgap gate



UFDG tended to underpredict high-V_{DS} current.

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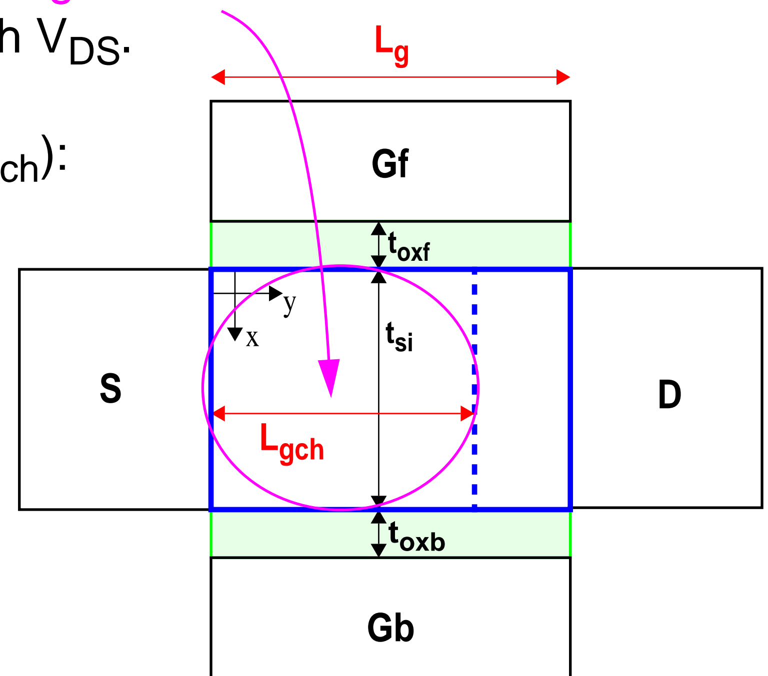
DICE Modeling in UFDG

Analogous to DIBL in weak inversion, drain-induced charge enhancement in the UTB/channel in strong inversion results from high V_{DS}.



2-D Poisson equation in gradual (n)channel ($0 \le y \le L_{gch}$):

$$\Delta Q_{ch}(y) = -\varepsilon_{Si}\int_0^{t_{Si}}\left(\frac{\partial^2}{\partial x^2}\Delta\phi(x,y)\right)dx - \varepsilon_{Si}\int_0^{t_{Si}}\left(\frac{\partial^2}{\partial y^2}\Delta\phi(x,y)\right)dx \ .$$

pinch-off tendency

DICE: $\Delta Q_{ch}^{DICE} \cong -\varepsilon_{Si} t_{Si} \frac{2V_{DS(eff)}}{L_{gch}^2}$

where $V_{DS\,(eff)}$ ($\cong V_{DS(sat)}$) is effective bias at $y = L_{gch}$.

(For $V_{DS} < V_{DS(sat)}$, $V_{DS(eff)} \rightarrow V_{DS}$ and $L_{gch} \rightarrow L_g$.)

$Q_{ch}(y) \rightarrow Q_{ch}(y) + \Delta Q_{ch}^{DICE}$ in UFDG formalism (which modifies/corrects the $L_{gch}(V_{GS}, V_{DS})$ and $V_{DS(eff)}(V_{GS}, V_{DS})$ characterizations) yields good accounting for DICE effects on current and terminal charges (and capacitances/transcapacitances). Note that DICE is a beneficial short-channel effect; it enhances Q_{ch} and I_{DS} without significantly increasing C_G since ΔQ_{ch}^{DICE} is supported mainly by the drain.

DICE is unique and significant to (undoped) nanoscale DG MOSFETs, and it is enhanced by scaling!

$$\Delta Q_{ch}^{DICE} \cong -\varepsilon_{Si} t_{Si} \frac{2V_{DS(eff)}}{L_{gch}^2} \quad \text{vs.} \quad Q_{ch}(y = 0) \sim (C_{oxf} + C_{oxb})(V_{GS} - V_t)$$

tends to be significant because

high μ_{eff} $\Rightarrow$ short L_{gch} (which offsets low $V_{DS(eff)}$),

and increases with scaling because

L_{gch} scales faster than $V_{DS(eff)}$ (and probably t_{ox} and L_g and t_{Si}).

Further, $v_{sat(eff)} > v_{sat} \Rightarrow$ high $V_{DS(sat)} \Rightarrow$ more DICE.

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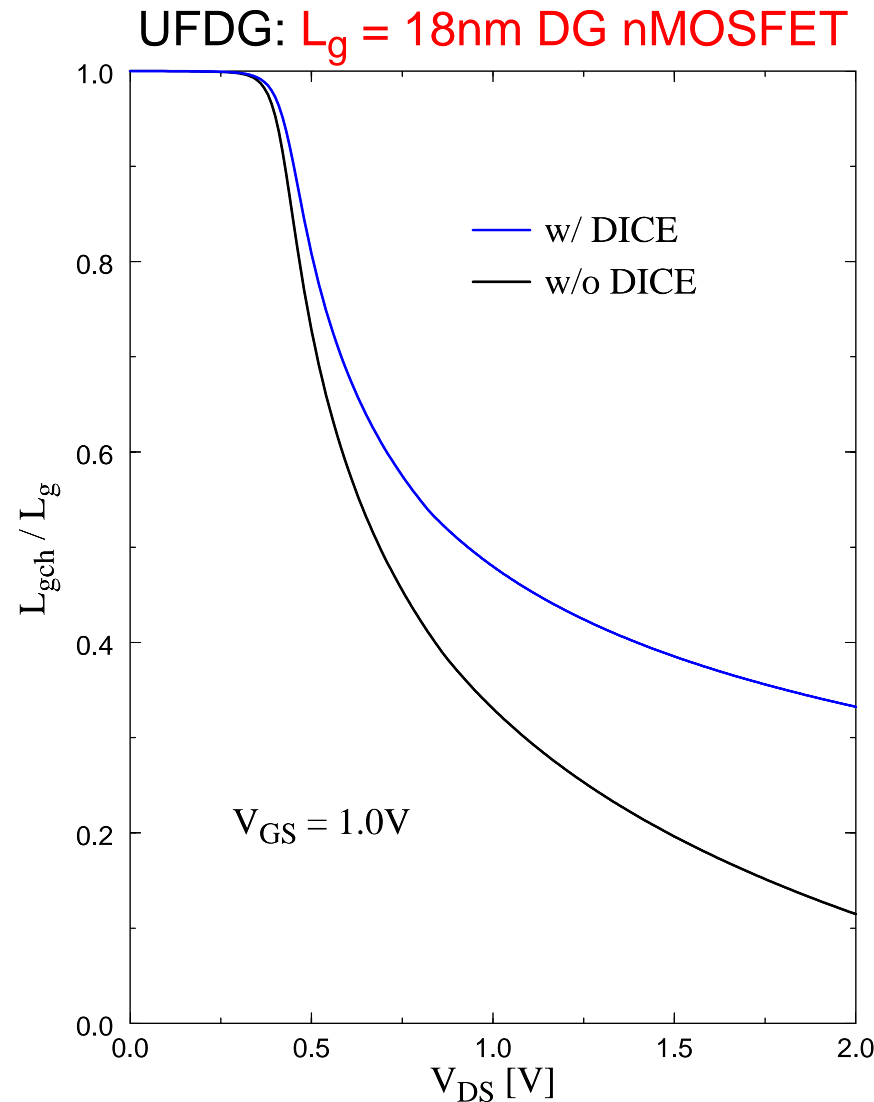
The DICE effect on L_{gch} is important:



The classical modeling of L_{gch}, or channel-length modulation, which affects current and charge, is invalidated by significant DICE.

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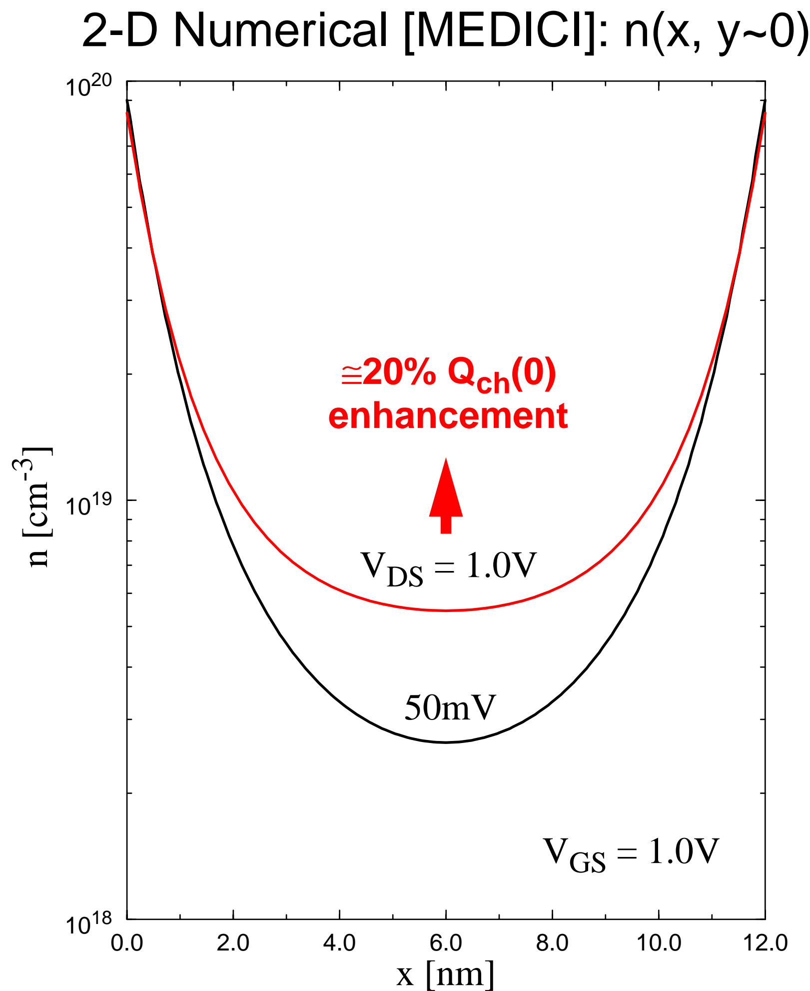
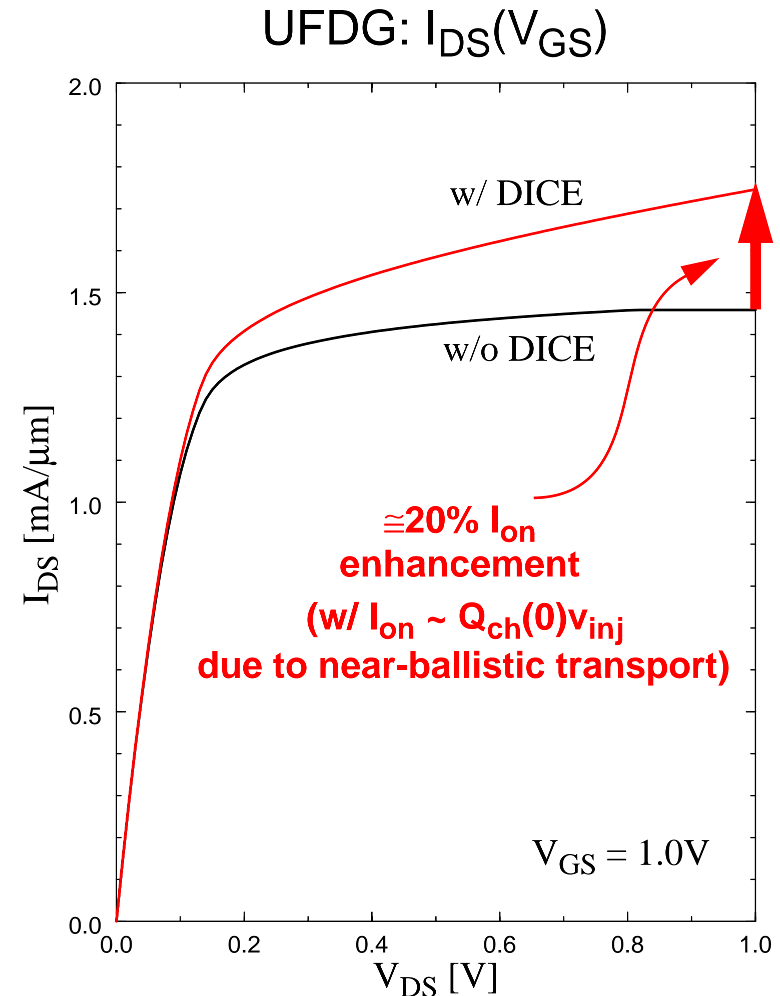
DICE Corroboration and Model Verification

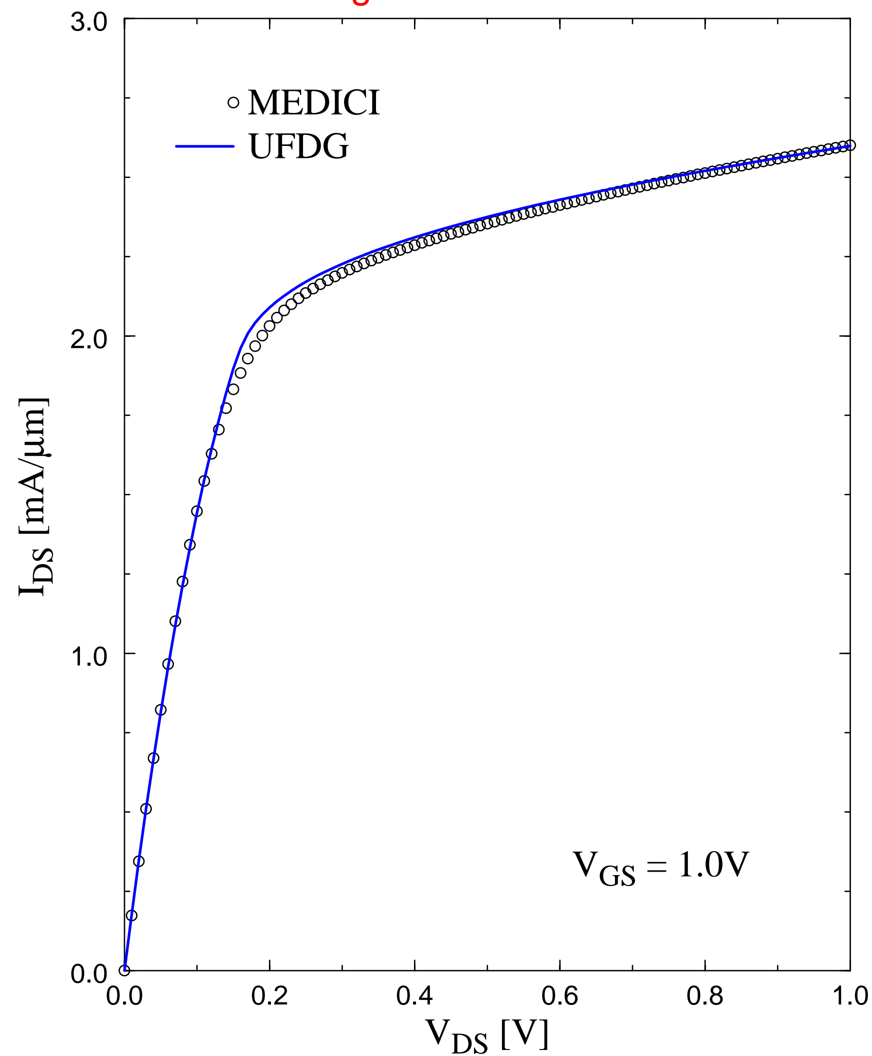
Simulations of *Simplified* L_g = 18nm DG nMOSFET; t_{Si} = 12nm





Numerical simulations predict DICE, verify UFDG model.

With I_{lim} turned off in UFDG, as (always) in MEDICI:



More corroboration!

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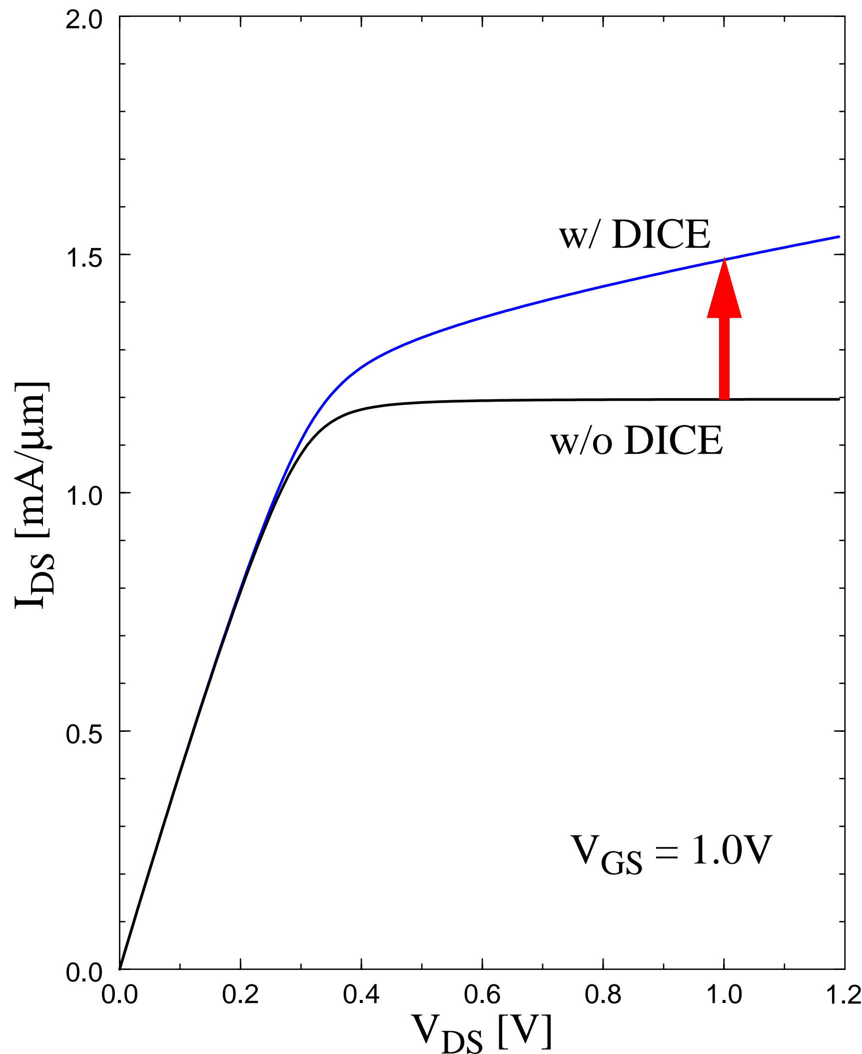
UFDG: Full Simulation of L_g = 18nm DG nMOSFET

(t_{Si} = 12nm, t_{ox}= 1.2nm, midgap gate)



24% I_{on} enhancement

(due directly to ΔQ_{ch}^{DICE} since current is near-ballistic, and greater than 20% because of velocity overshoot, even with nominal $R_{S/D}$)

The enhancement would be smaller if the current were not ballistic since it would be undermined some by the increase in L_{gch} caused by DICE.

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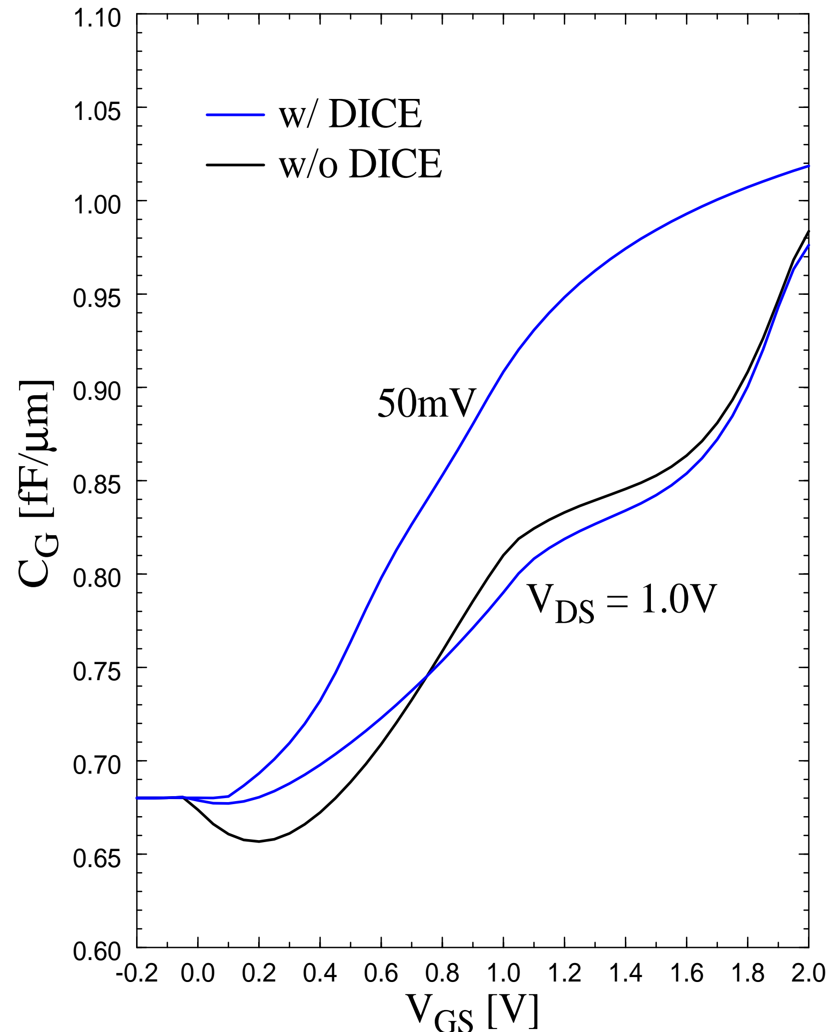
The gate capacitance is not affected significantly by DICE:

UFDG: L_g = 18nm DG nMOSFET



With the current near-ballistic, the UFDG charge modeling contains a degree of uncertainty since L_{gch} and $V_{DS(eff)}$ could be affected by I_{lim}.

Note that including DICE in the model tends to improve the moderate-inversion splining of terminal charges (Q_{Gf} + Q_{Gb} here) and channel current.

Does the enhanced I_{DS} without an increase in C_G translate to higher speed?

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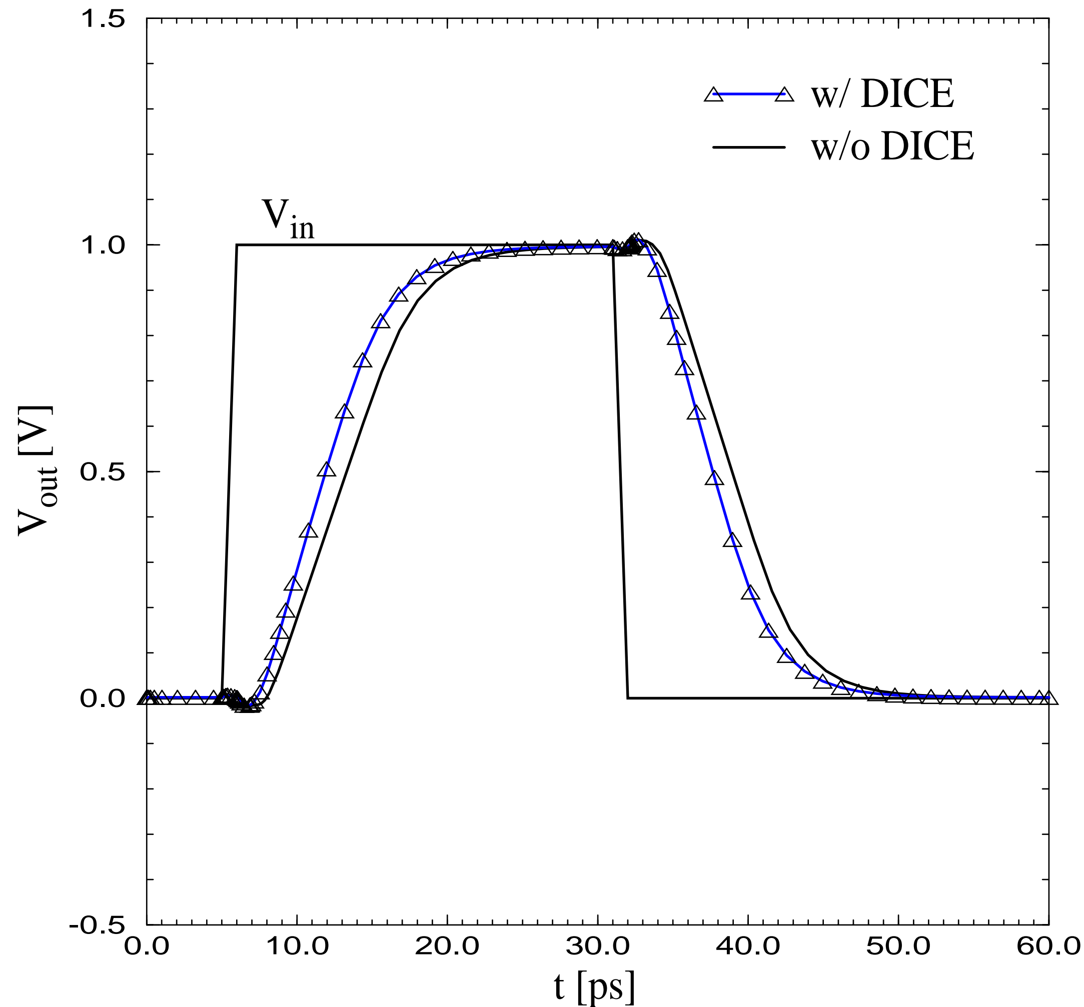
YES!

UFDG/Spice3:

two-stage CMOS inverter chain with L_g = 18nm DG MOSFETs; V_{DD} = 1.0V, C_{load} = 10fF



DICE decreases the average propagation delay by about 18%.

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Summary

❋ High carrier mobility in undoped nanoscale DG MOSFETs results in unique saturation-region, short-channel effects: significant and beneficial velocity overshoot and DICE, which are now physically accounted for in UFDG.

❋ The high mobility and velocity overshoot should result in ballistic carrier transport for $L_g < \cong 20$nm.

❋ DICE should be enhanced by device scaling; it increases current and improves nanoscale DG CMOS speed, especially when the current is near the ballistic limit.